

Cover Sheet	1
Block Diagram/Clock Map/Power Map	2-4
Intel LGA775 CPU	5-7
Intel Lakeport - MCH	8-11
Intel ICH7 - PCI & DMI & CPU & IRQ	12
Intel ICH7 - LPC & ATA & USB & GPIO	13
Intel ICH7 - POWER	14
Clock - RTM 876-660	15
LPC I/O - Fintek 71882FG	16
Azalia - ALC888	17
LAN REALTEK RTL8100C	18
DDR II System Memory	19
DDR II VTT Decoupling	20
PCI EXPRESS X16 Slot	21
PCI Slot 1 & 2 & 3	22
JMicron 1394	23
ATA33/66/100 IDE & SATA Connectors	24
VGA Connector	25
USB Connectors	26
ATX Connetcor & Front Panel	27
FWH	28
ACPI CONTROLLER MS7	29
VRM 11	30

MS-7398

Version 0A

CPU:

Intel Prescott (L2=2MB) - 3.4G & Above
 Intel Cendar Mill (65nm) - 3.73G & Above
 Intel Smithfield (90nm Dual core)
 Intel Conroe (65W Dual core)

System Chipset:

Intel Lakeport - MCH (North Bridge)
 Intel ICH7R (South Bridge)

On Board Chipset:

BIOS -- FWH EEPROM
 HD -- ALC888
 LPC Super I/O -- F71882FG
 LAN-- REALTEK RTL8111B/C Co-lay RTL8101E
 CLOCK -- ICS954519

Main Memory:

DDR II *4 (Max 2GB)

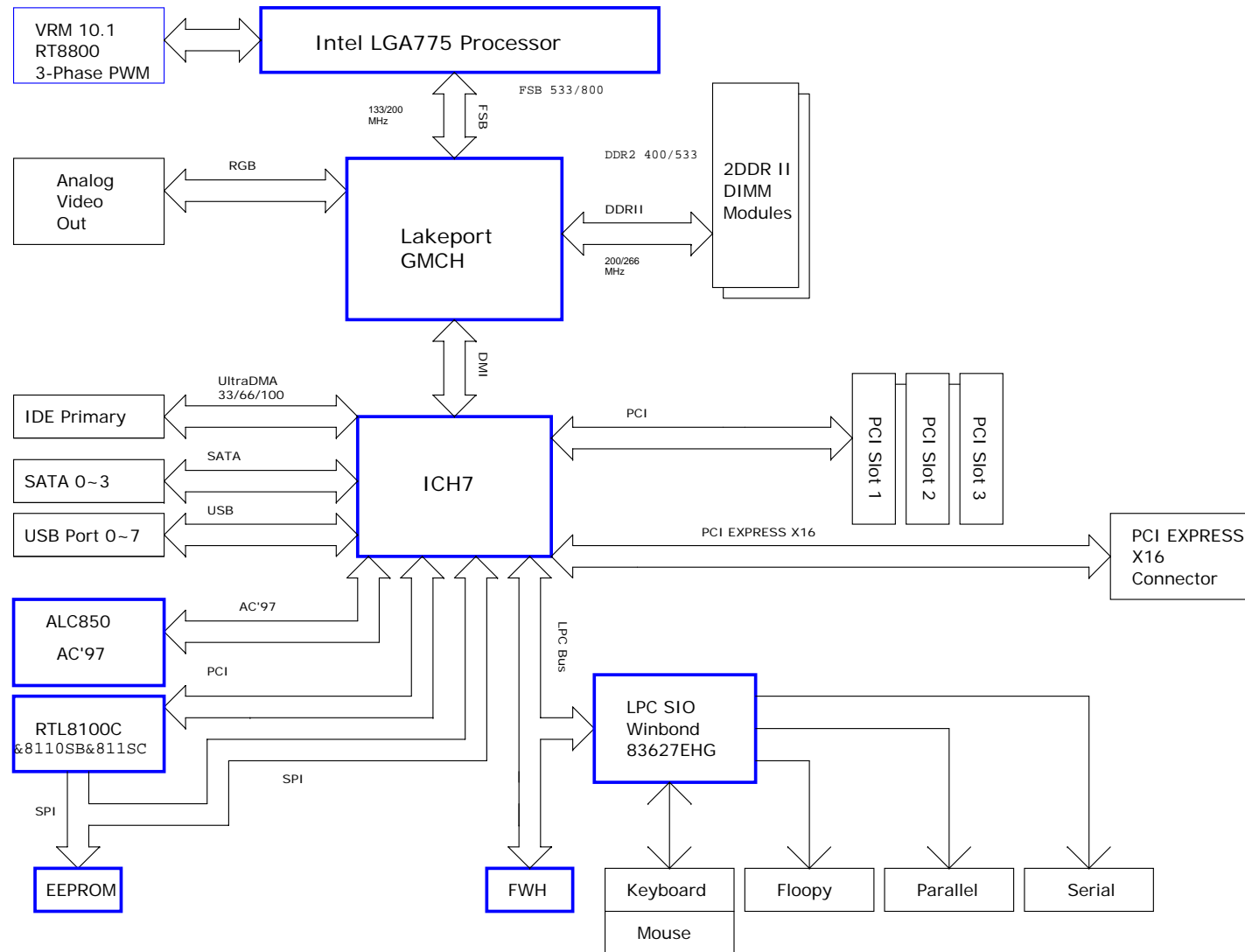
Expansion Slots:

PCI2.3 SLOT * 3
 PCI EXPRESS X16 SLOT

RICH PWM:

Controller: 3 PHASES

Block Diagram

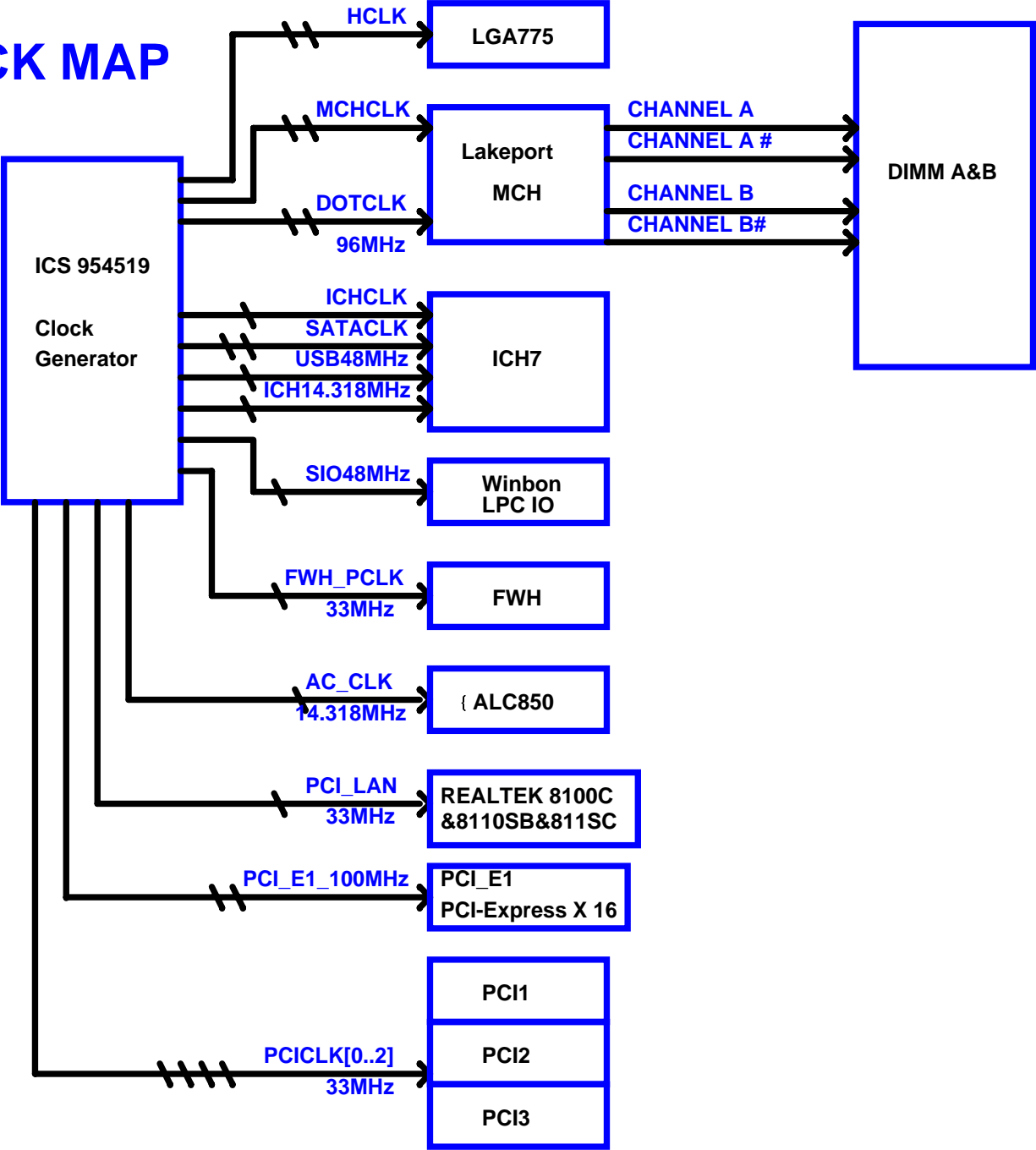


MICRO-STAR INT'L CO.,LTD

MS-7398

Size Custom	Document Description BLOCK DIAGRAM	Rev 0A
Date: Monday, July 09, 2007	Sheet 2 of 32	

CLOCK MAP

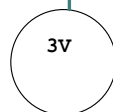


INTEL 775		
0.8375V - 1.6000V Core	-	125A
1.2V FSB Vtt	-	5.3+0.8=6.1A

NB-945GC		
+1.3V REGULATOR	-	8.81 A
+1.3VDUAL REGULATOR	-	25 mA
+1.8V REGULATOR	-	2.4 A
+3.3V REGULATOR	-	621 mA
+3.3V DUAL	-	163mA
RTC (G3)	-	3 mA

Audio		
3.3V AUDIO	-	40mA
5V AUDIO	-	200mA

SPI		
+3.3V (S0,S1)	-	30mA



ISL6322		
VCCP	VRM 11	
0.8375V-1.6000V	125A	
4-Phase Switch		

W83310DS		
VTT_DDR		
0.9V	Linear	1.2A

Regulator		
V_FSB_VTT		
5.3A+0.85A=	6.1A	
VCC1_3		
1.35V	Linear	8.81A
5VUSB_REAR/FRONT		
5V	Linear	2A / 3A
5VSB	400mA / 600mA	
5VDIMM		
5V		9.34A
5VSB		225mA

uP7706 Regulator		
3VDUAL		
3.3V		1.7A

uP7707 Regulator		
1_3VDUAL		
1.35V		25mA

uP6103 Regulator		
VCC_DDR		
1.8V	Switch	22.21A (S3)

5VAudio	+5VR	800mA
---------	------	-------

+12V	
ATX 2x2	

+12V	+5V	+3.3V	+5VSB
ATX POWER			

DDR DIMM & TERMINATOR		
0.9V VTT_DDR	-	1.2A
1.8V VCC_DDR (S0,S1)	-	9.4A
1.8V VCC_DDR (S3)	-	400mA

PCI Express x16 slot (X1)		
+12V	-	5.5 A
+3.3Vaux (wake)	-	375mA
+3.3Vaux (no wake)	-	20mA
+3.3V	-	3.0A

PCI Express x1 slot (X1)		
+12V	-	0.5 A
+3.3Vaux (wake)	-	375mA
+3.3Vaux (no wake)	-	20mA
+3.3V	-	3.0A

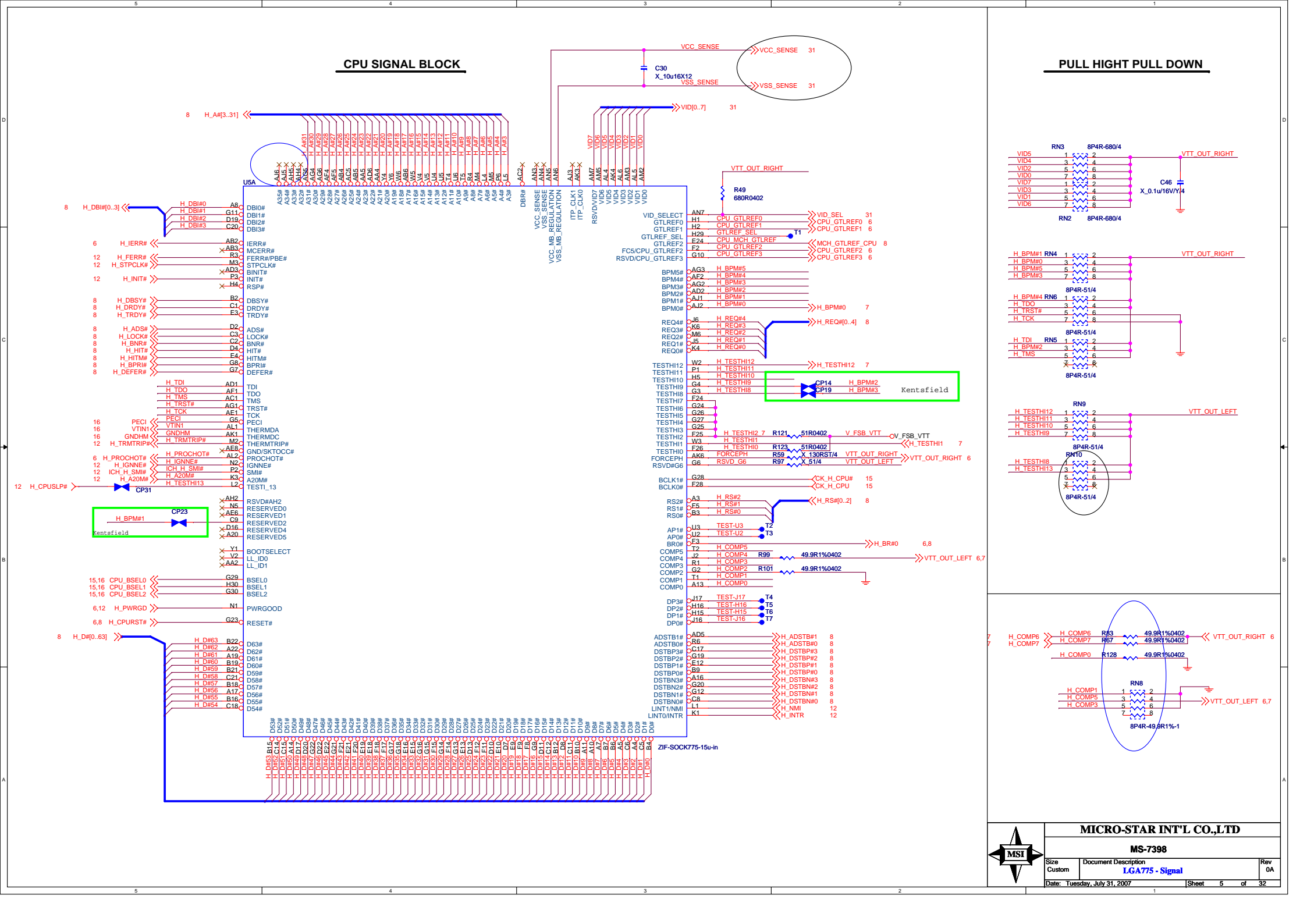
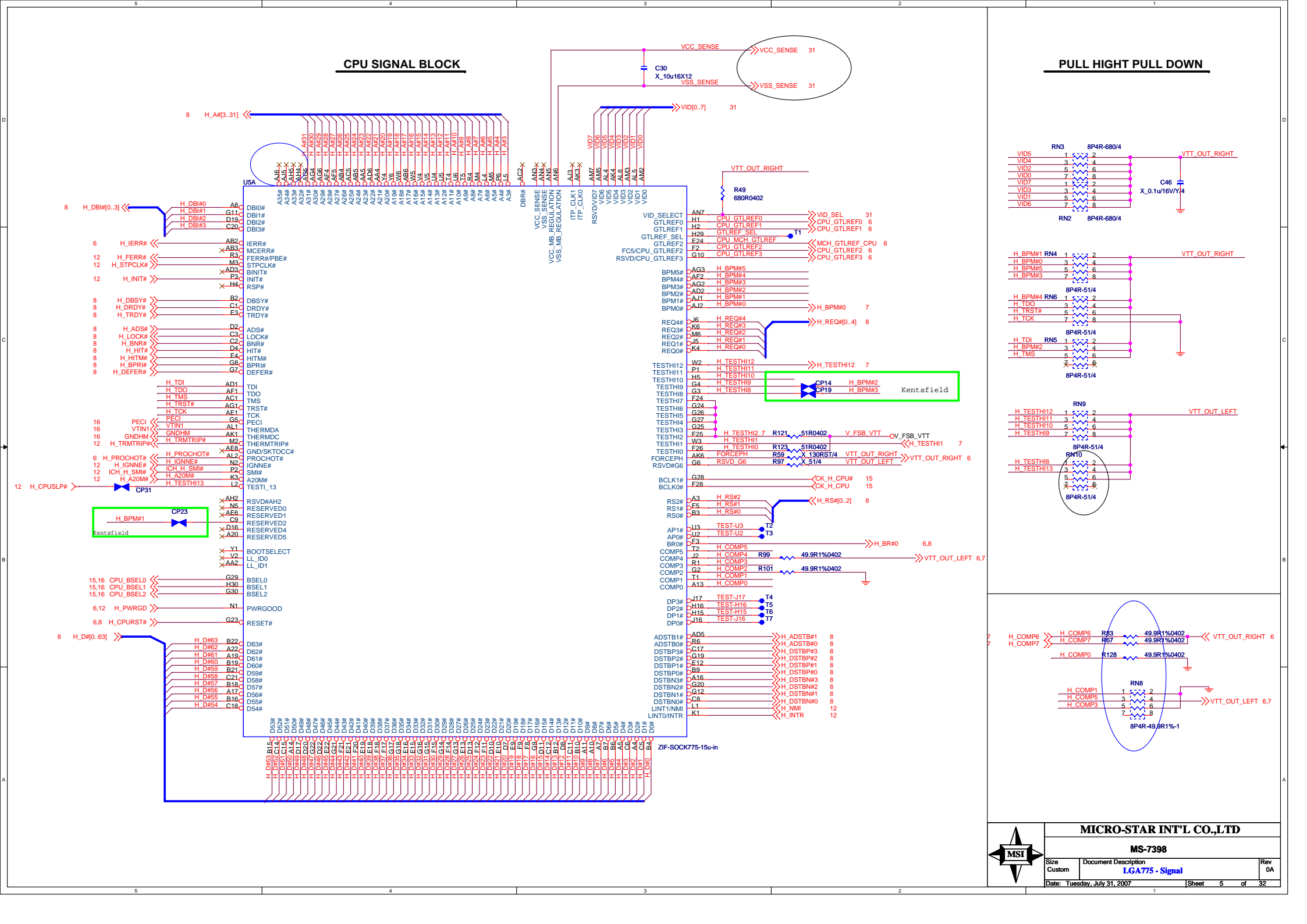
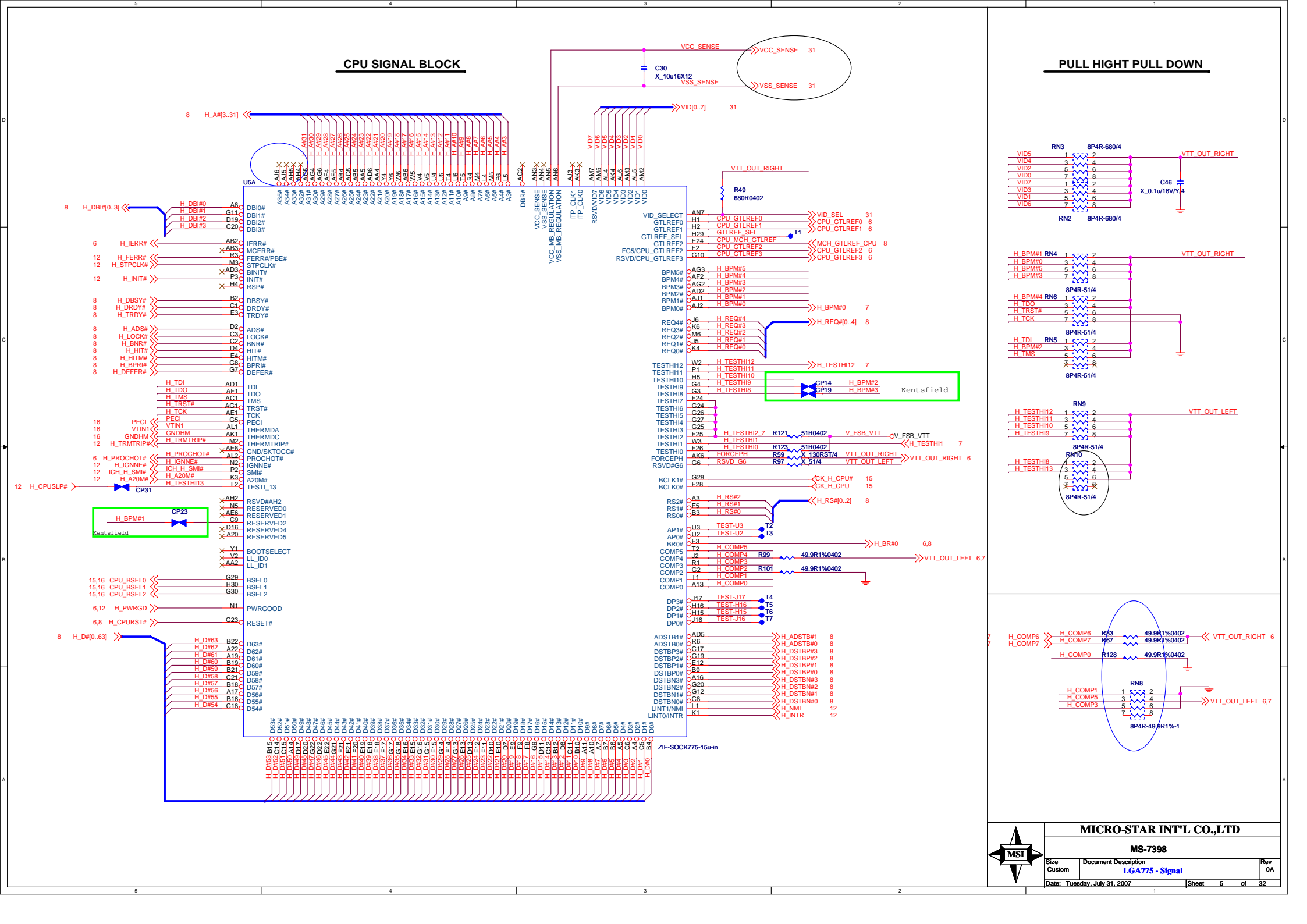
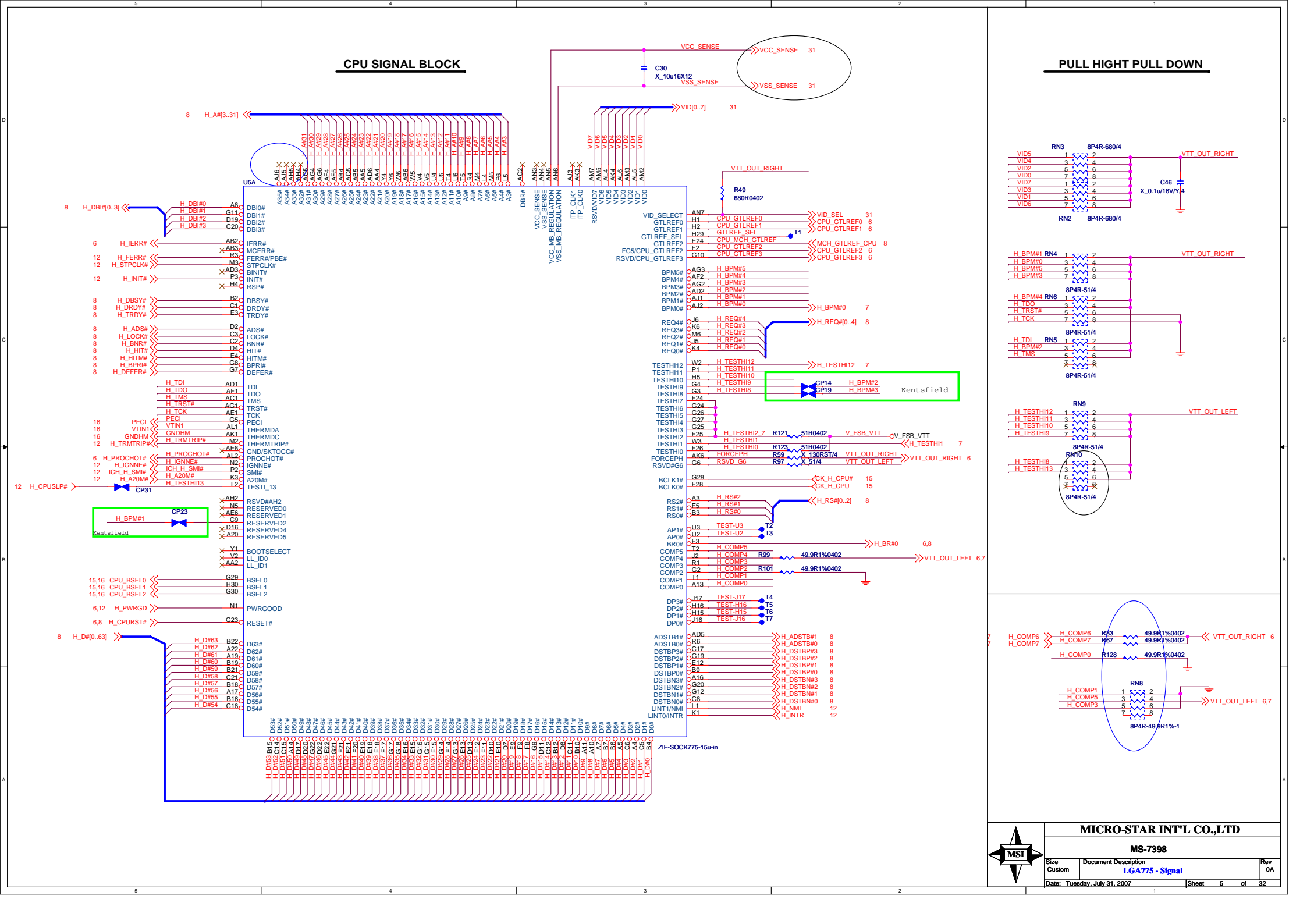
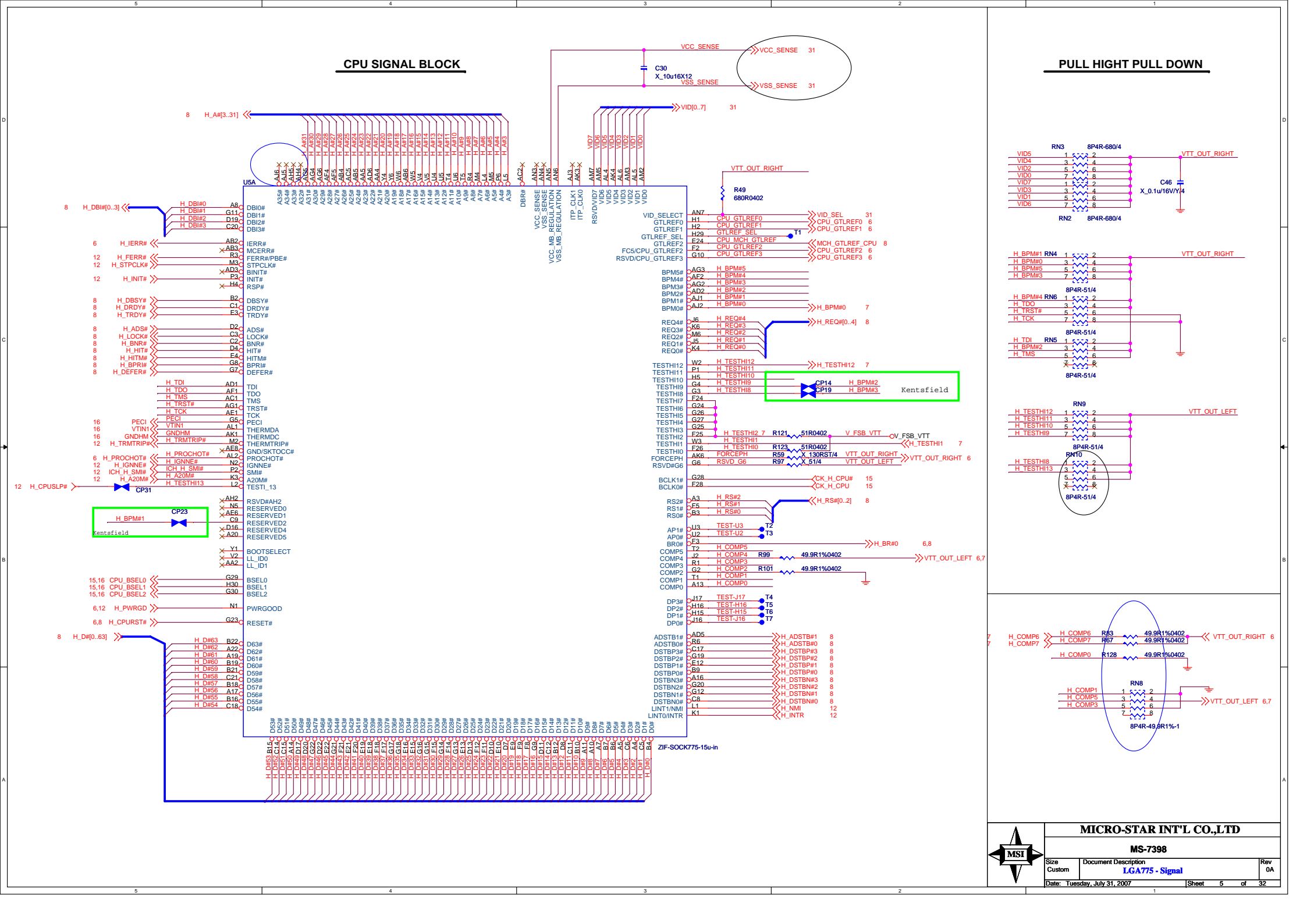
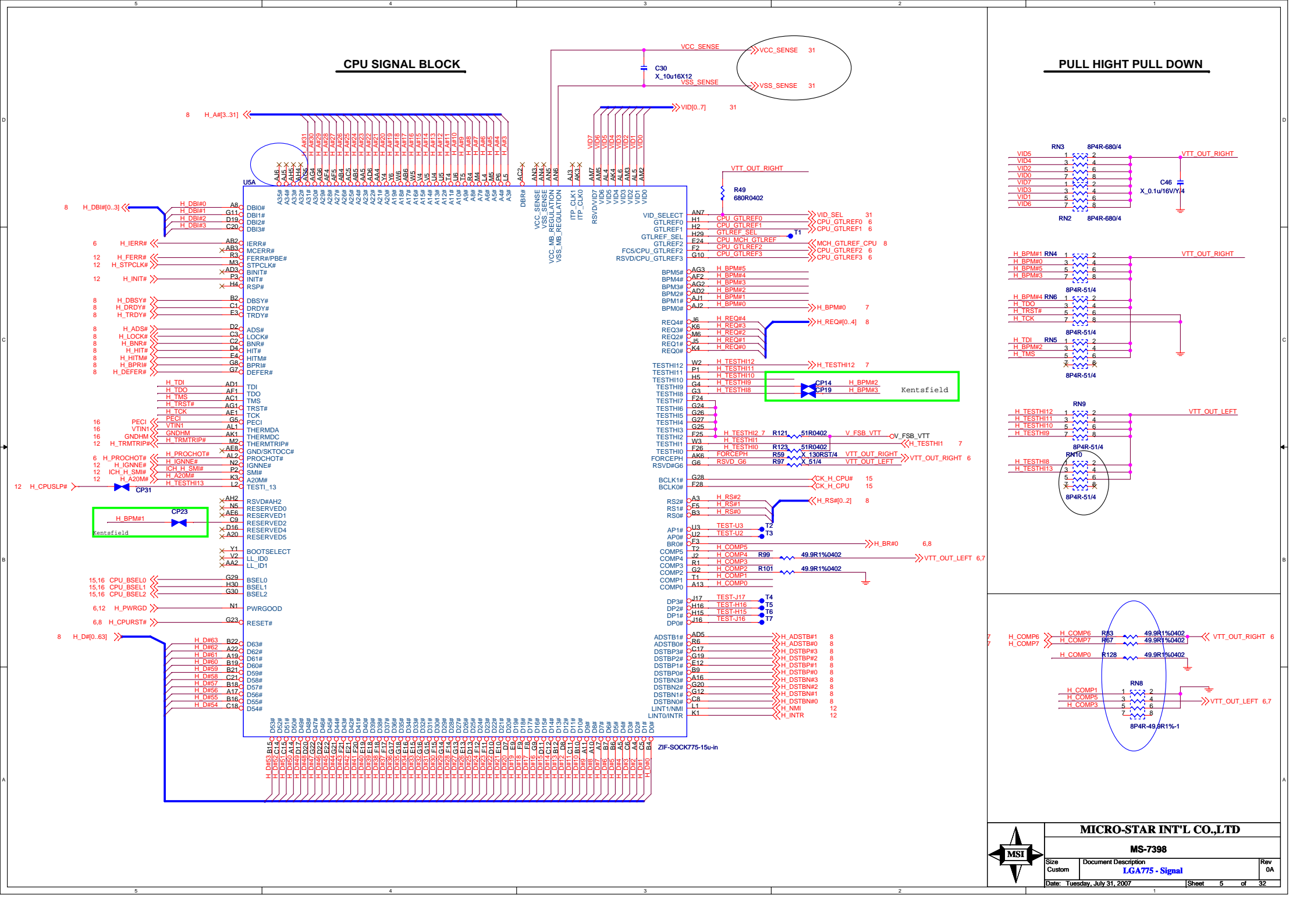
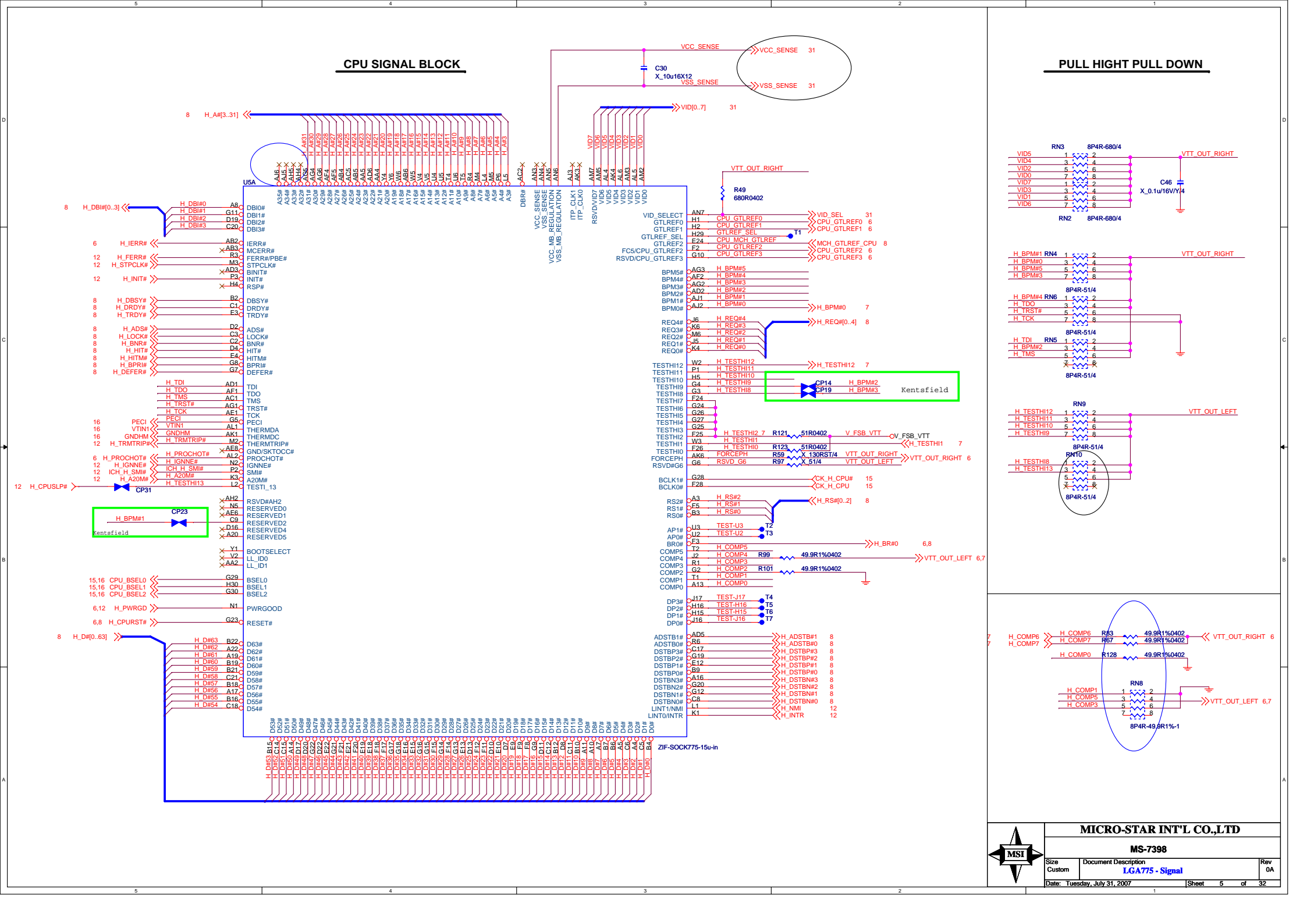
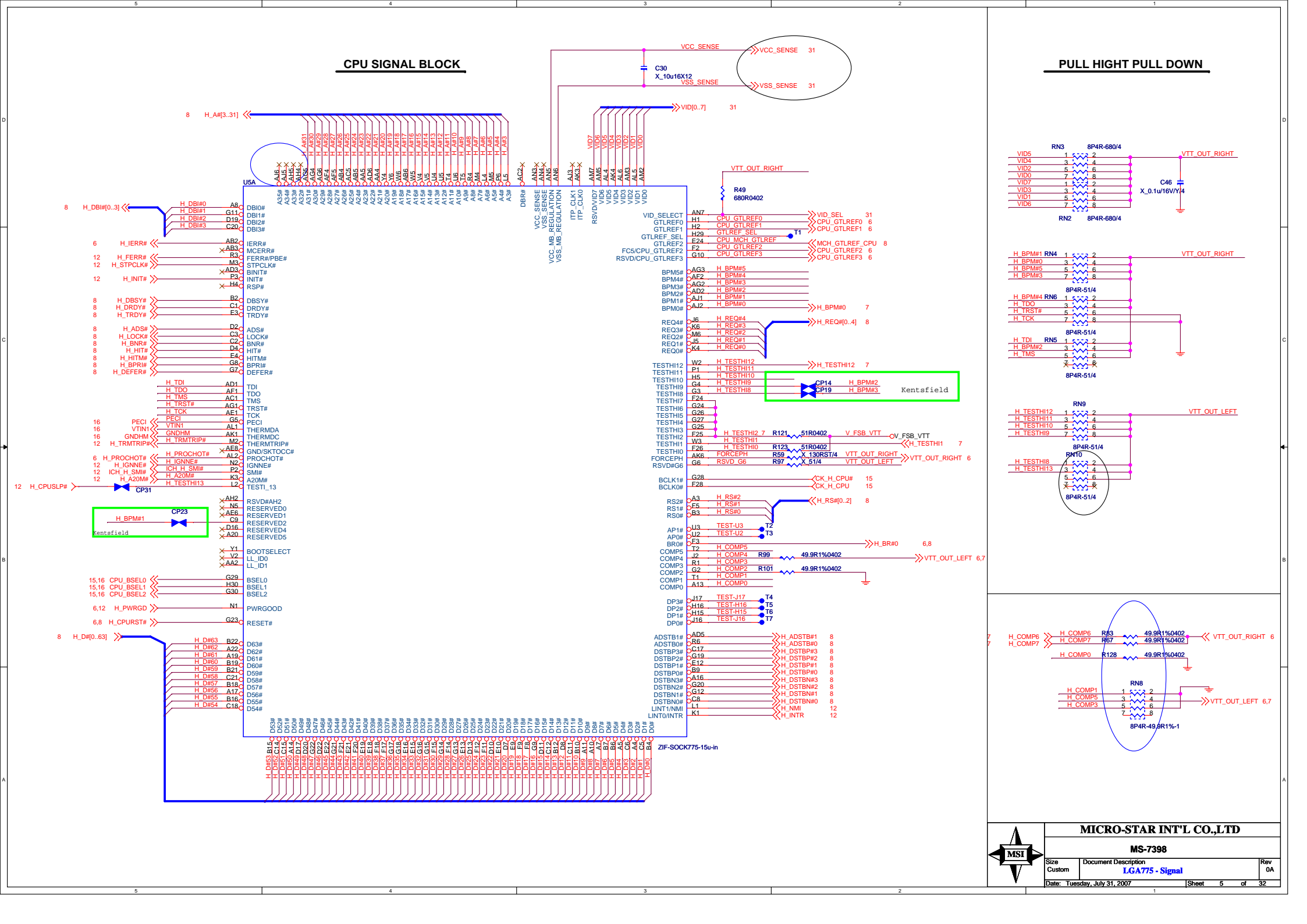
PCI slot x2		
+3.3Vaux (wake)	-	750mA
+3.3Vaux (no wake)	-	40mA
+3.3V	-	15.2A
+5V	-	10A
+12V	-	1.0A

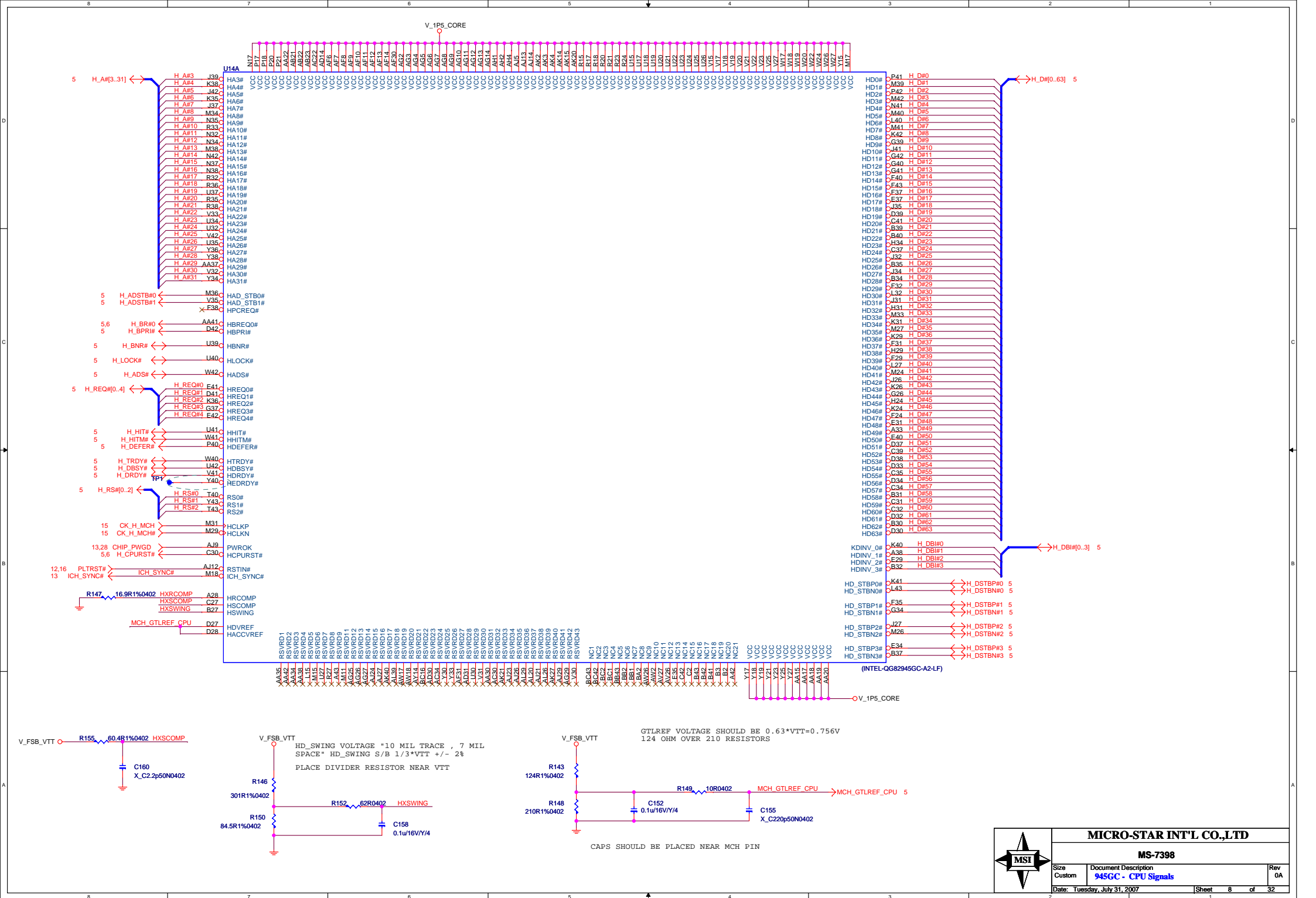
USB		
+5V (S0,S1)	-	5.0A
+5V (S3)	-	25mA

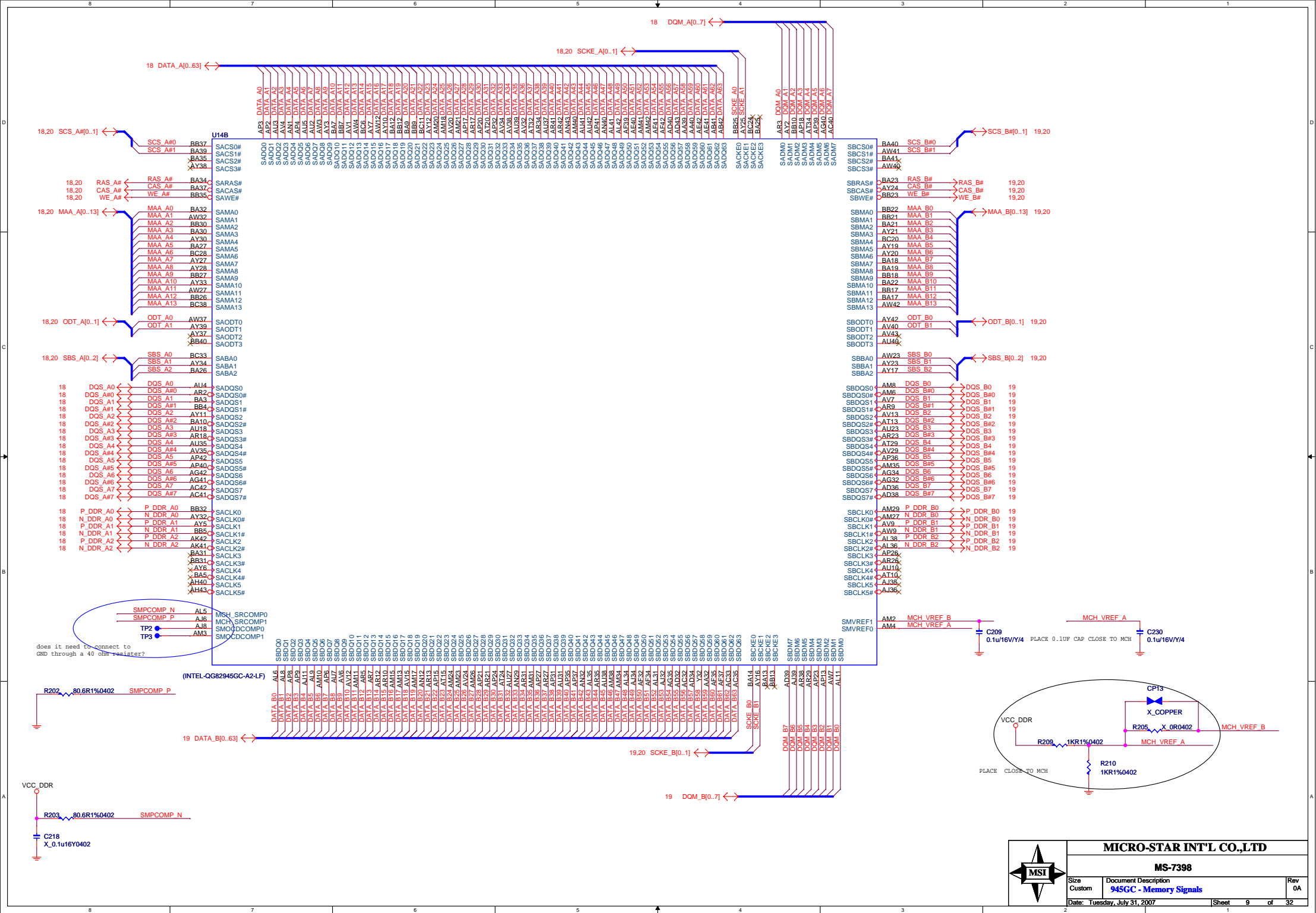
PS2		
+5V (S0,S1)	-	345mA
+5V (S3)	-	2.0mA

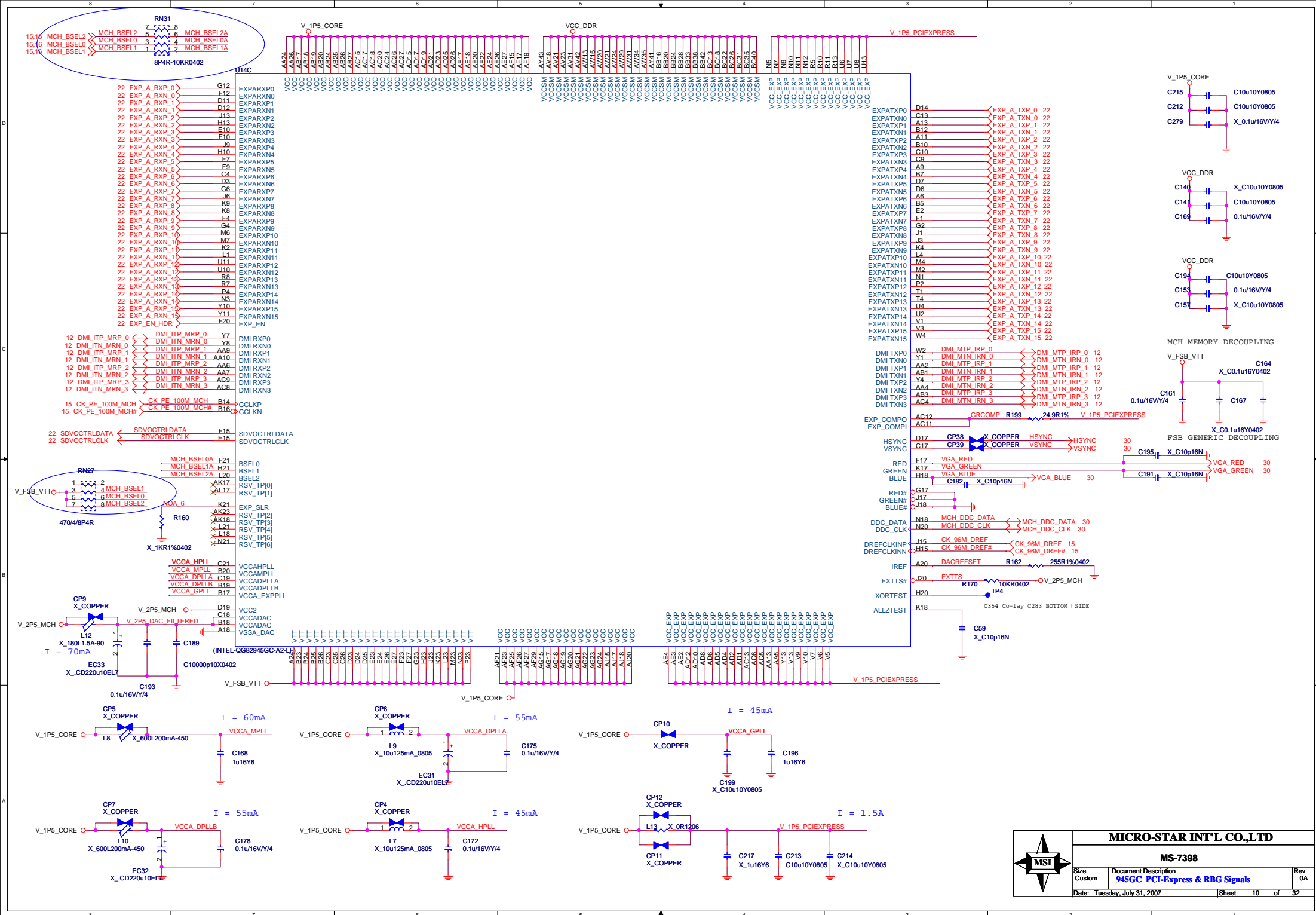


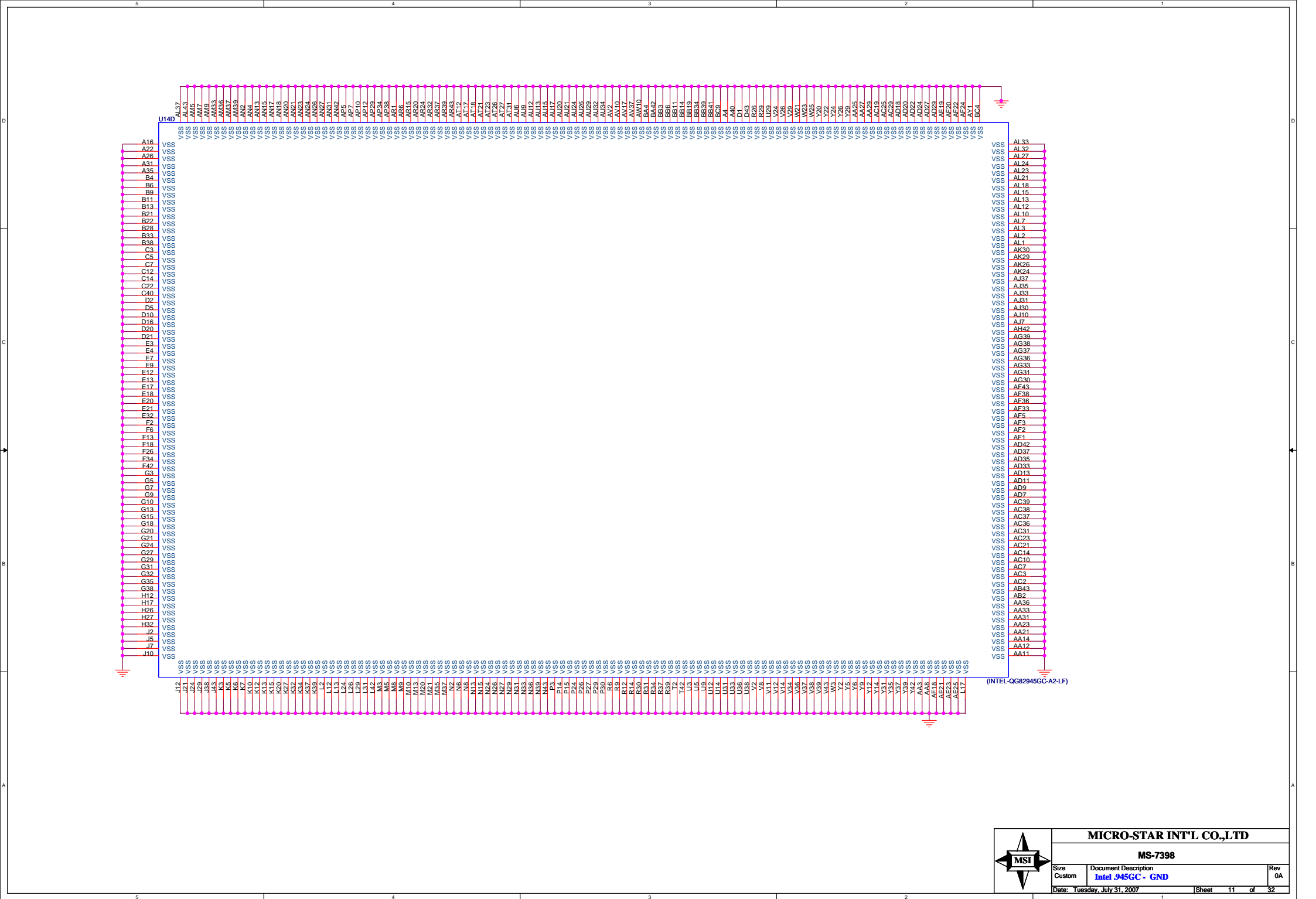
MICRO-STAR INT'L CO.,LTD			
MS-7398			
Size Custom	Document Description	Rev 0A	
POWER MAP			
Date: Tuesday, July 10, 2007	Sheet 4 of 32		

[illegible][illegible][illegible][illegible]



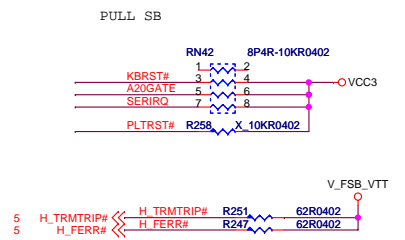
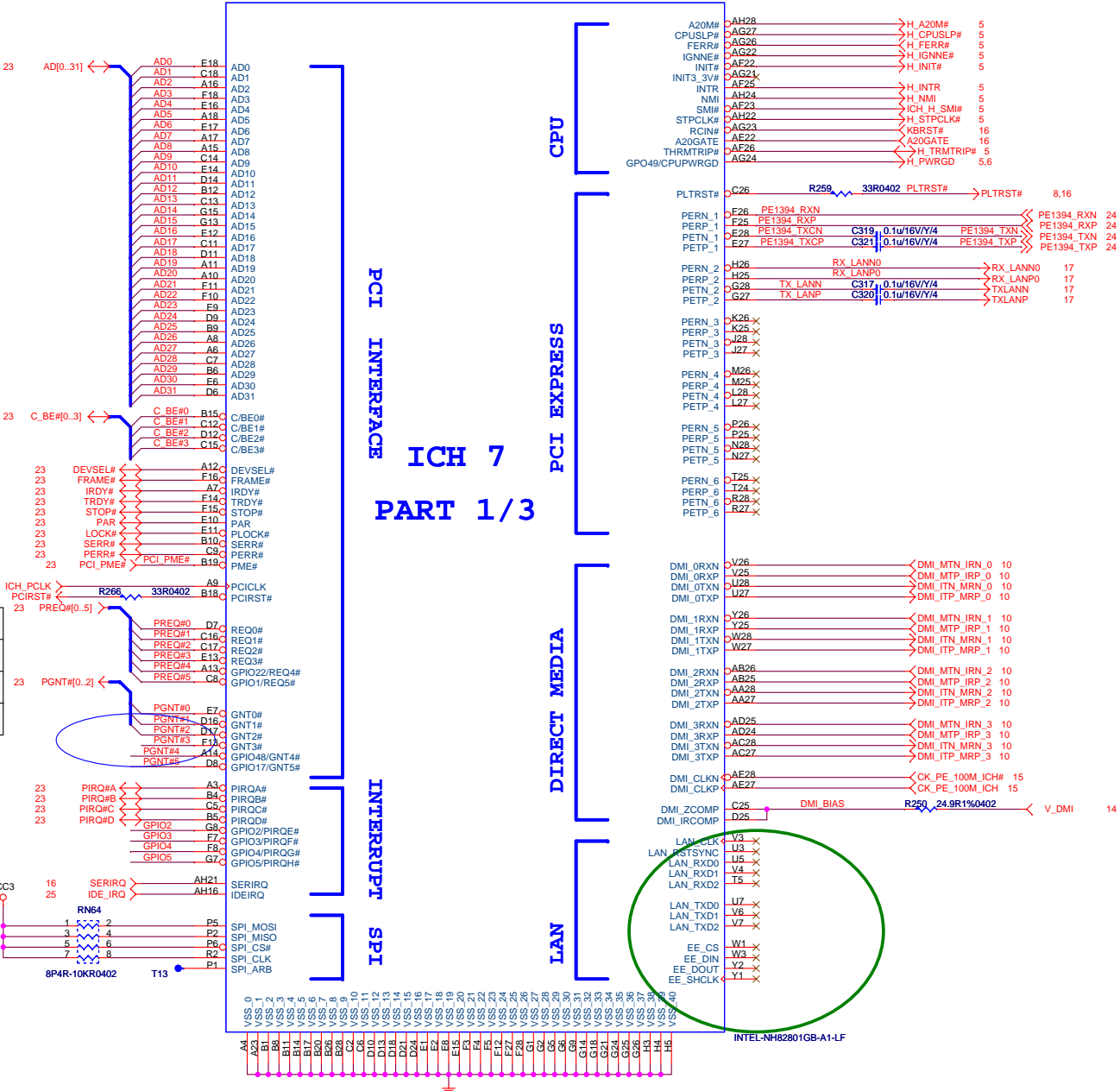
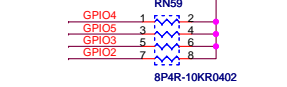
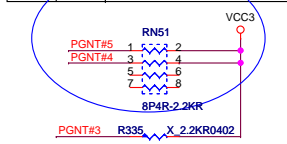


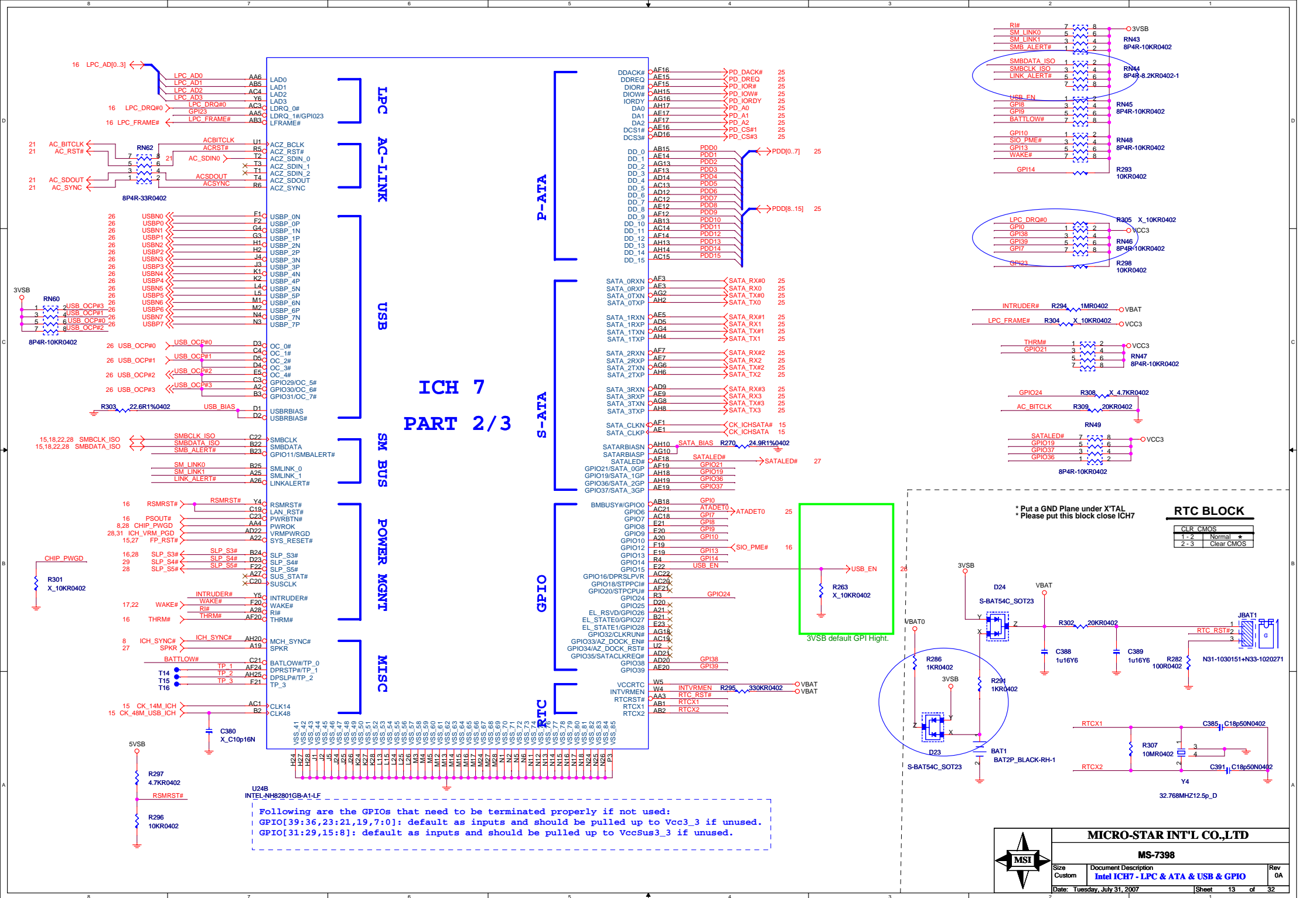


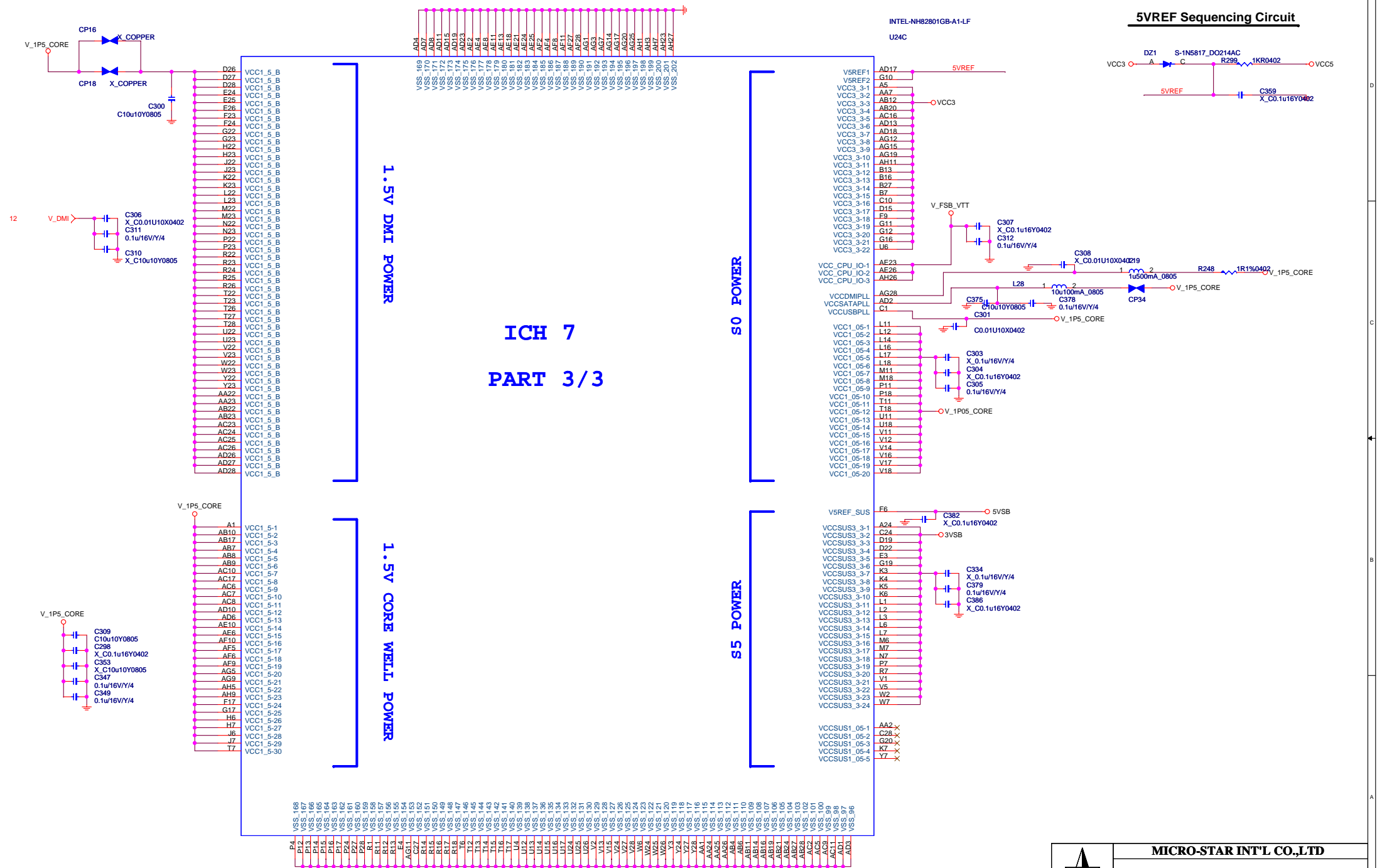


ICH 7 PART 1/3

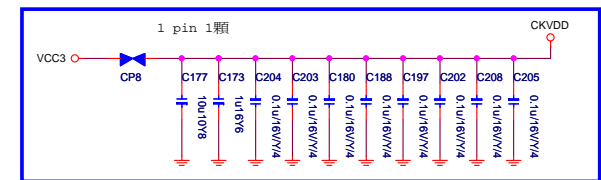
GNT5#	GNT4#	ROUTING
0	1	Flash Cycles Routed to SPI
1	0	Flash Cycles Routed to PCI
1	1	Flash Cycles Routed to LPC







The timing diagram shows two signals, CLK_X1 and CLK_X2, which are both labeled as 14.318MHz. The signals are represented by red lines. CLK_X1 is a square wave with a period of approximately 68.7ns. CLK_X2 is a square wave with a period of approximately 68.7ns. The signals are shown for a duration of 10ns. The signals are connected to a circuit component labeled Y1, which is a buffer or inverter. The input of Y1 is connected to CLK_X1, and the output is connected to CLK_X2. The circuit also includes two capacitors, C165 and C166, both labeled as 30pF. C165 is connected to the input of Y1, and C166 is connected to the output of Y1. The signals are shown for a duration of 10ns.



SEL 0 R158 10KR0402 CKV/DD

SEL 1 R186 10KR0402

SEL_P4/K8# R159 X 10K/4 CKV/DD

Internal pull high,
no need to stuff

Clock Generator Power Good Block

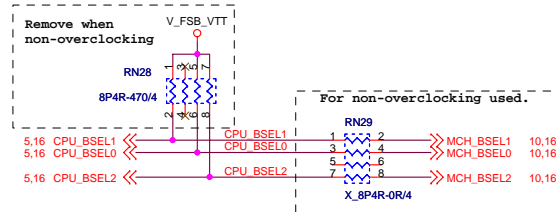
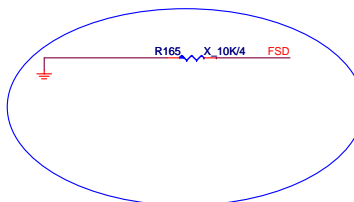
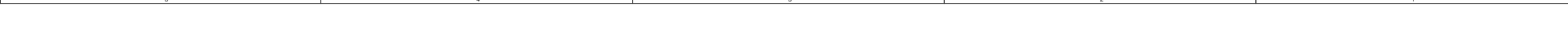
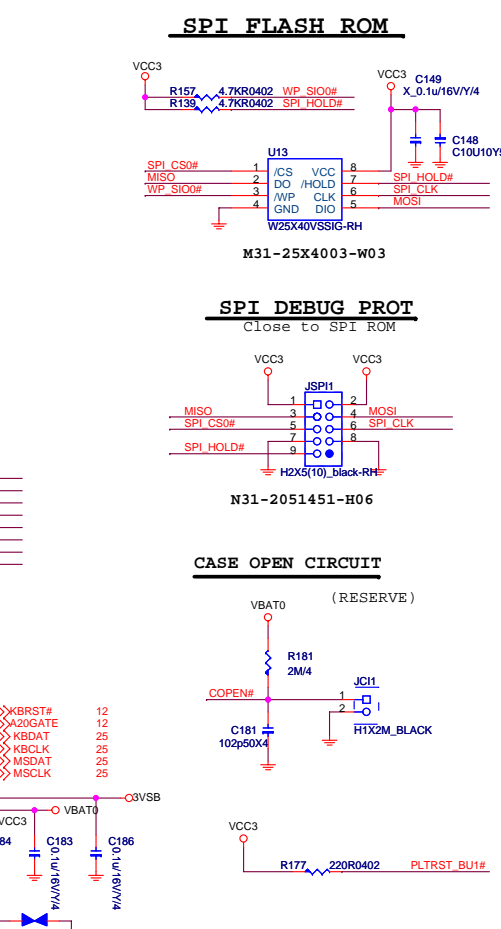
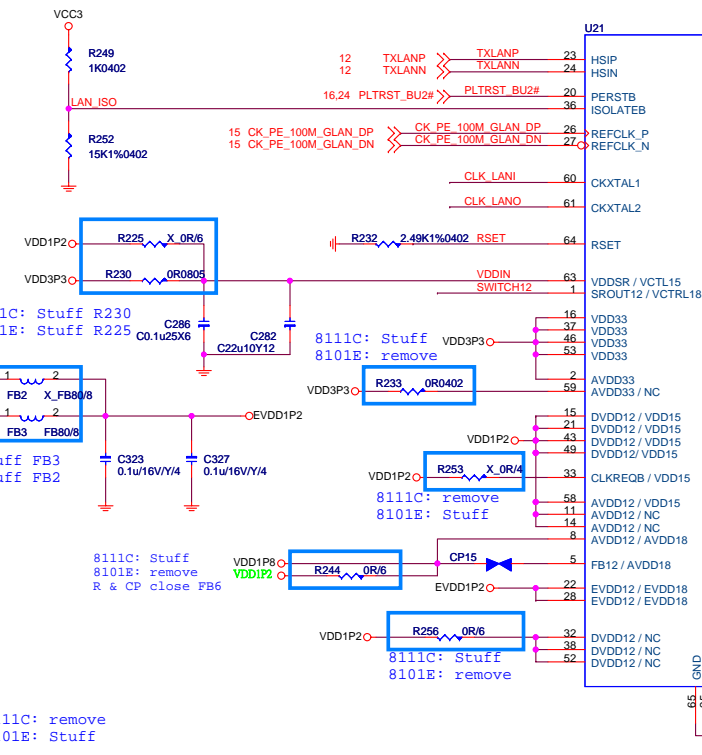
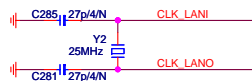


Diagram of the 8P4R-1KR0402 component showing its pin configuration. The component is an 8-pin package with pins numbered 1 through 8. Pin 1 is labeled CPU_BSEL2, Pin 2 is FSC, Pin 3 is CPU_BSEL1, Pin 4 is FSB, Pin 5 is CPU_BSEL0, Pin 6 is FSA, Pin 7 is CPU_BSEL0, and Pin 8 is FSA. The component is labeled RN30 and 8P4R-1KR0402.

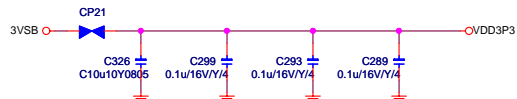
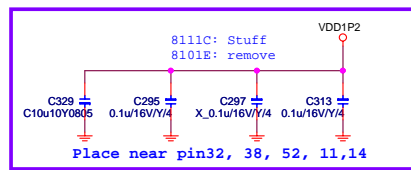
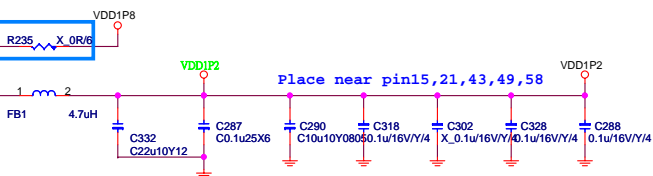


Size Custom	Document Description CLK-RTM 876-660	Rev 0A
Date: Tuesday, July 31, 2007		Sheet 15 of 32

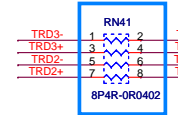




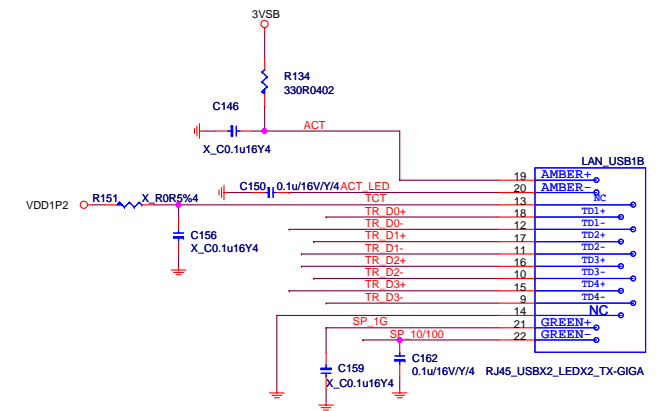
8111C: remove
8101E: Stuff



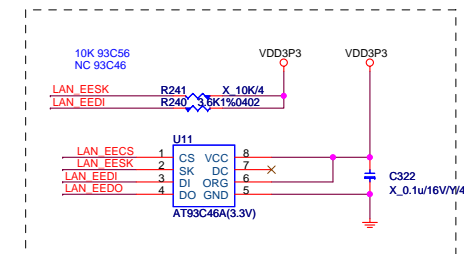
8111C: Stuff
8101E: remove

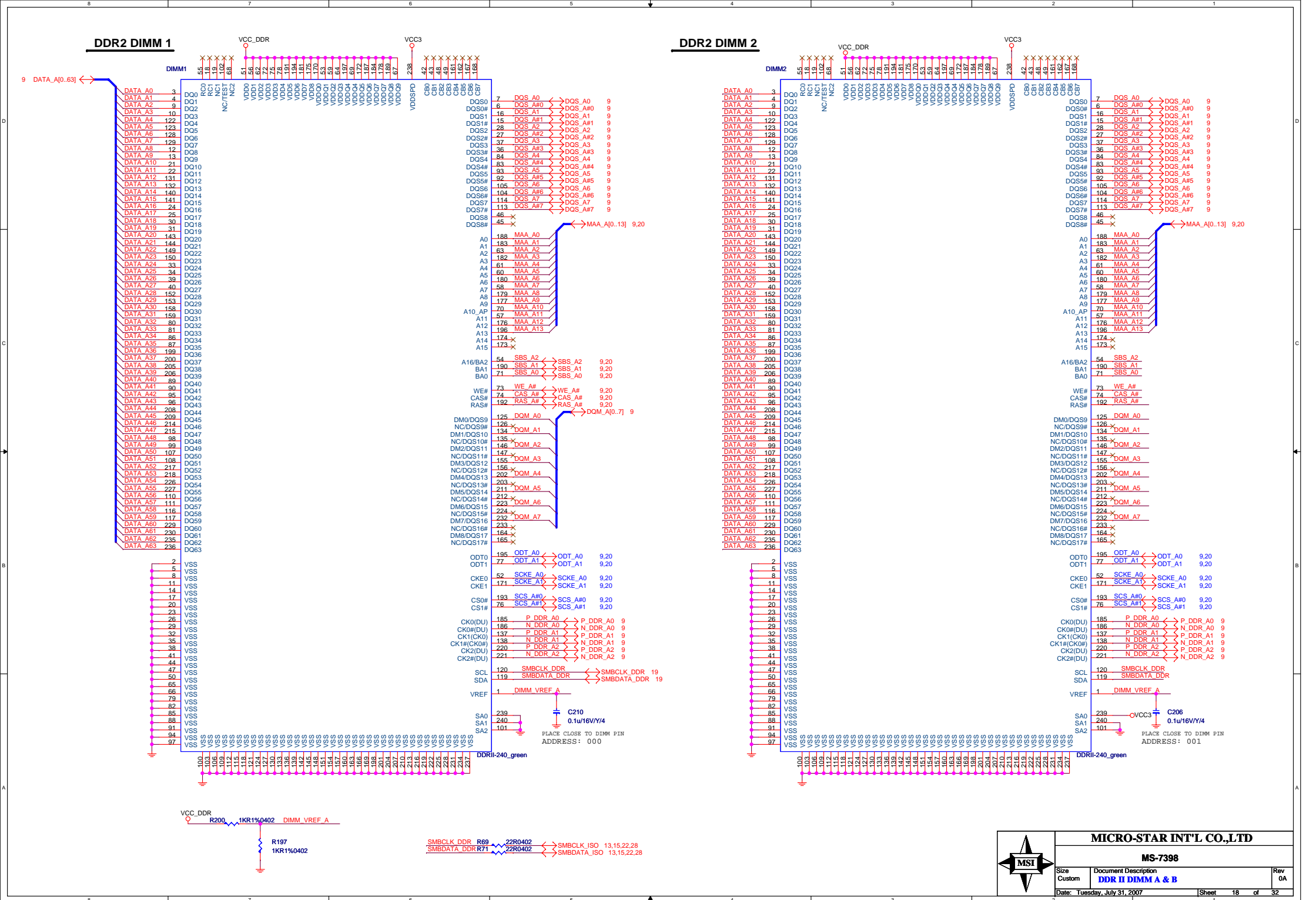


8111C: Stuff
8101E: remove

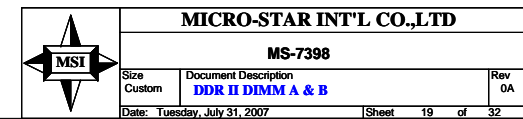
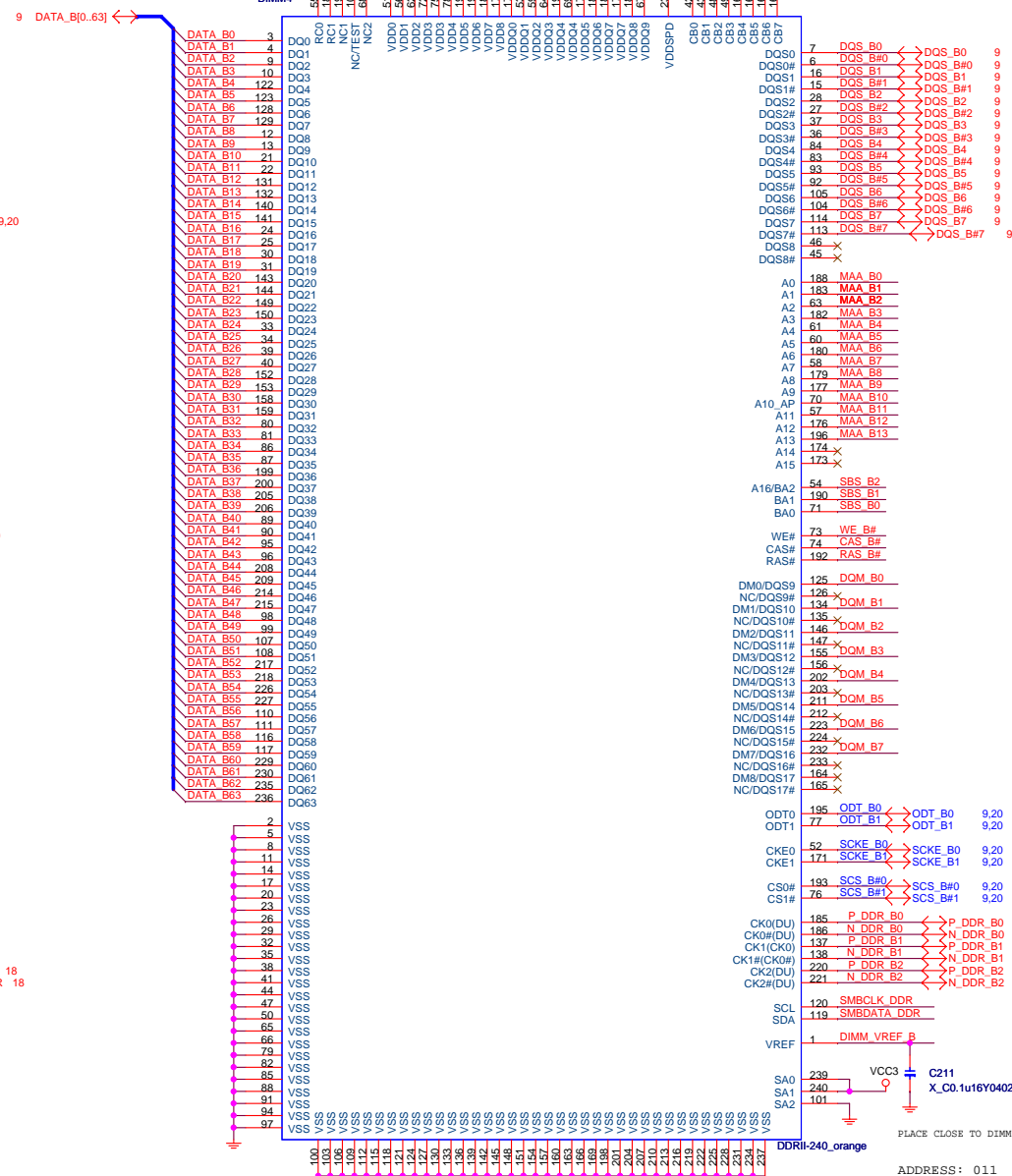


N58-22F0181-S42

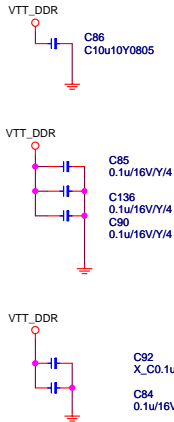




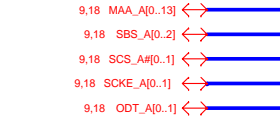
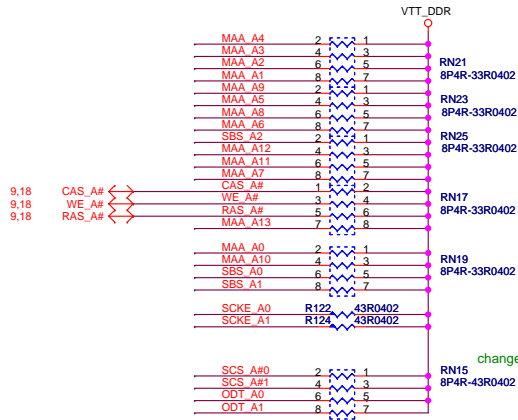
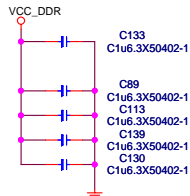
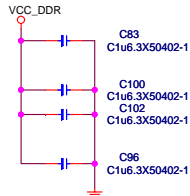
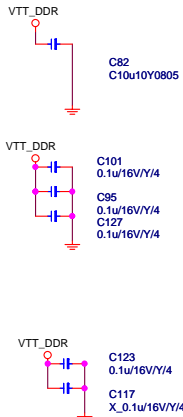
DDR2 DIMM 4



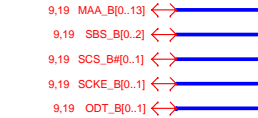
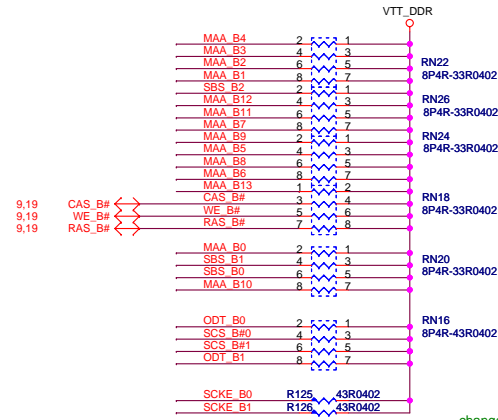
CHANNEL A V_SM_VTT DECOUPLING CAPS



CHANNEL B V_SM_VTT DECOUPLING CAPS



change RN



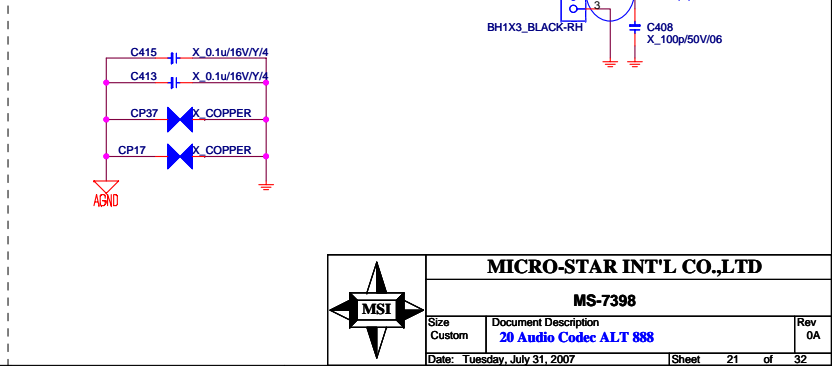
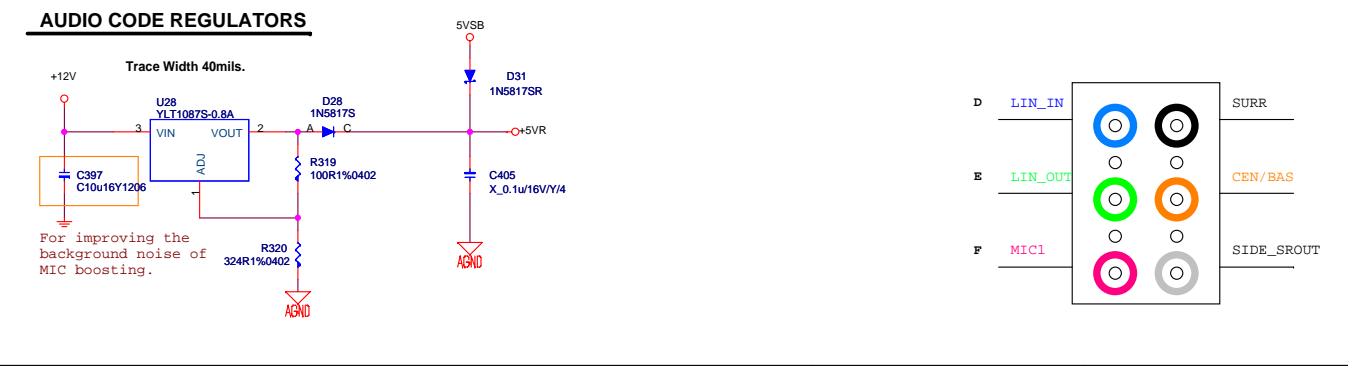
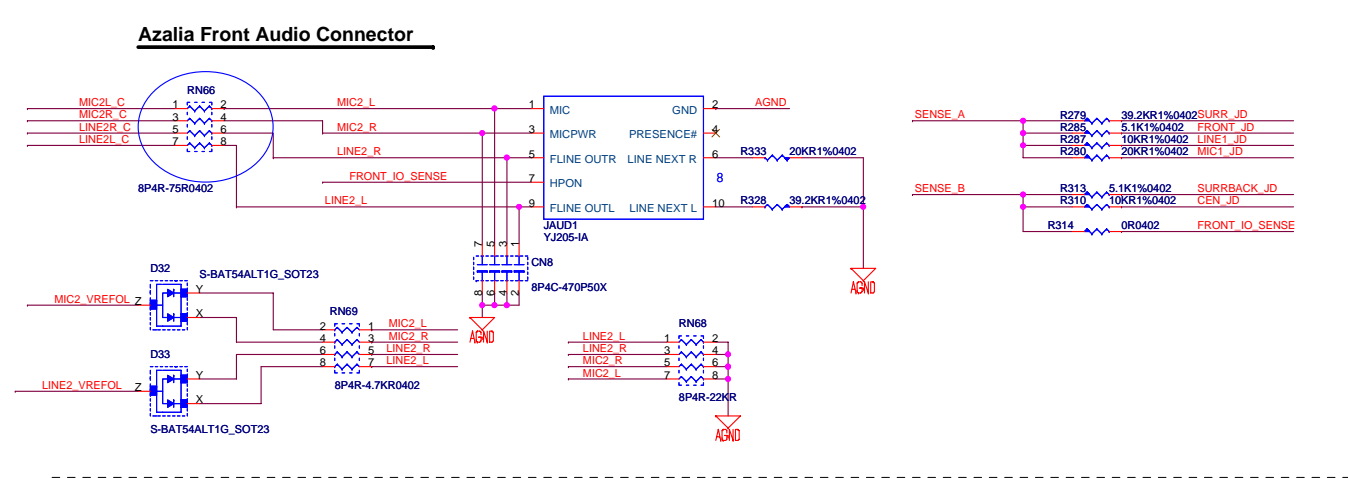
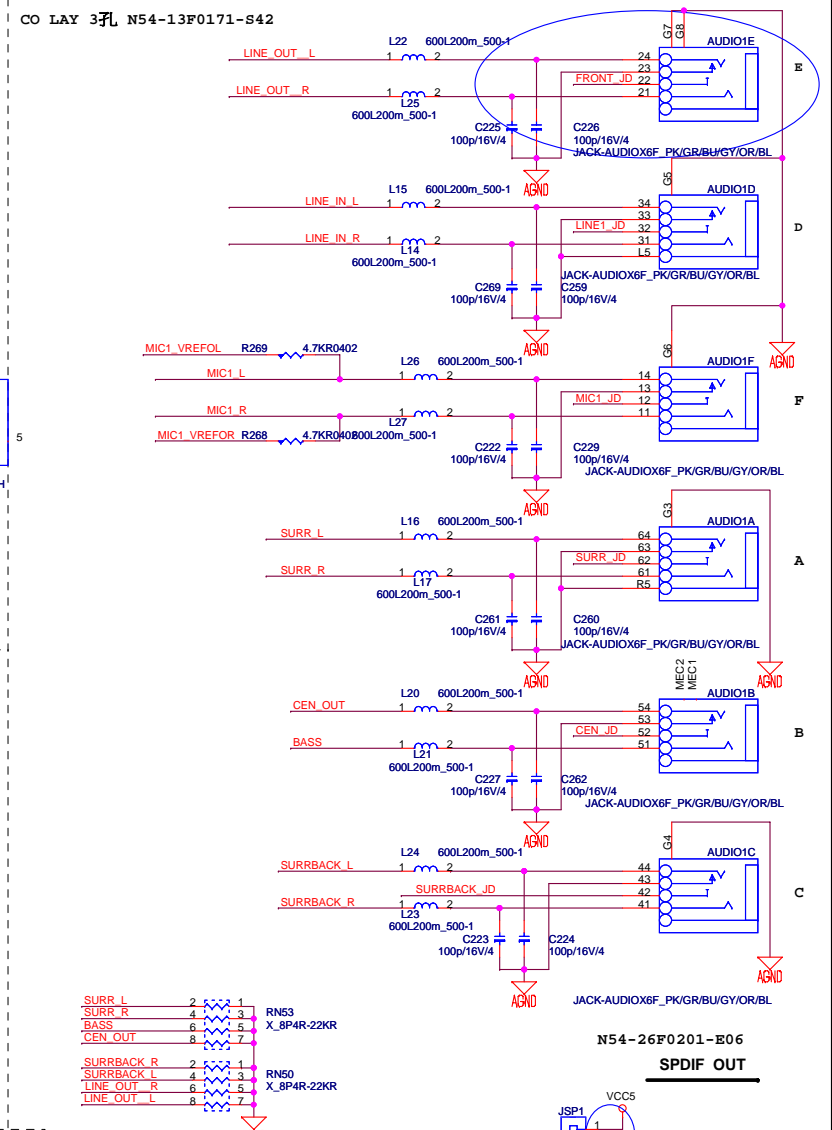
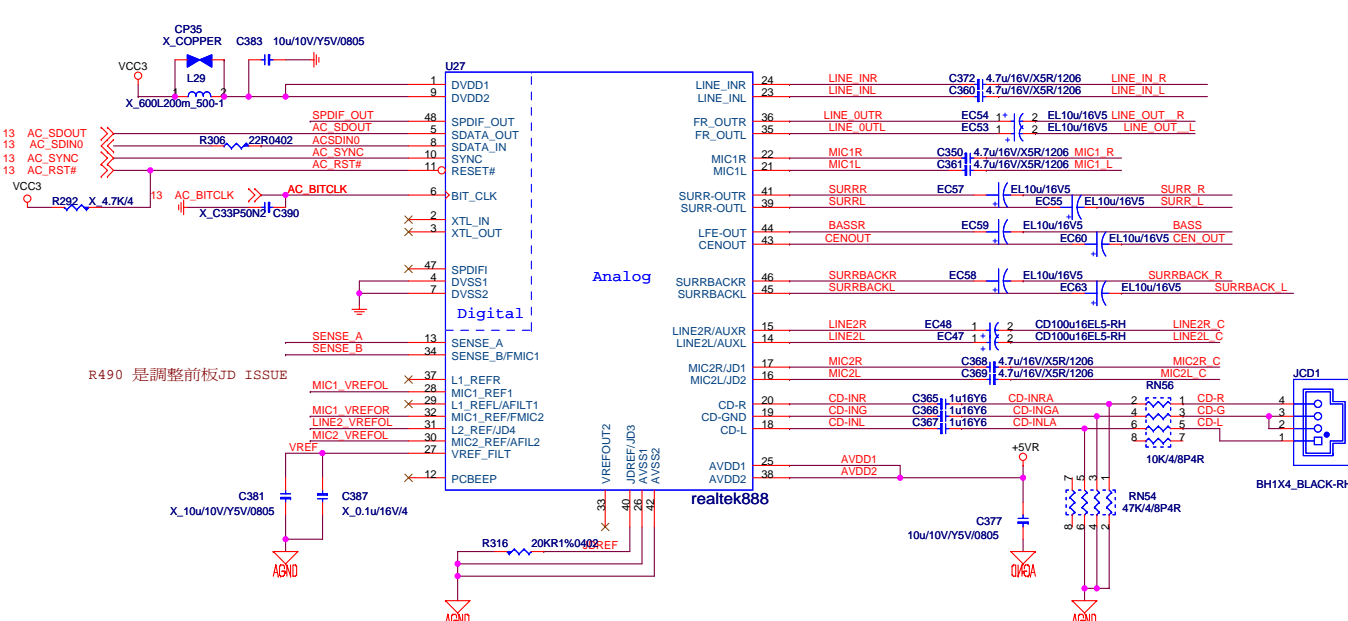
change RN

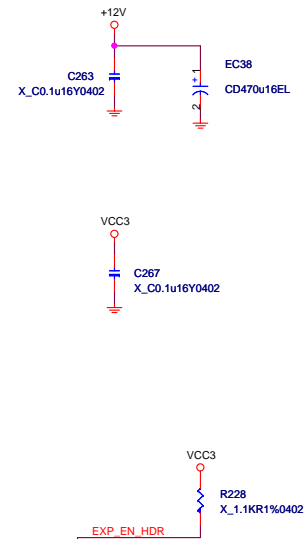
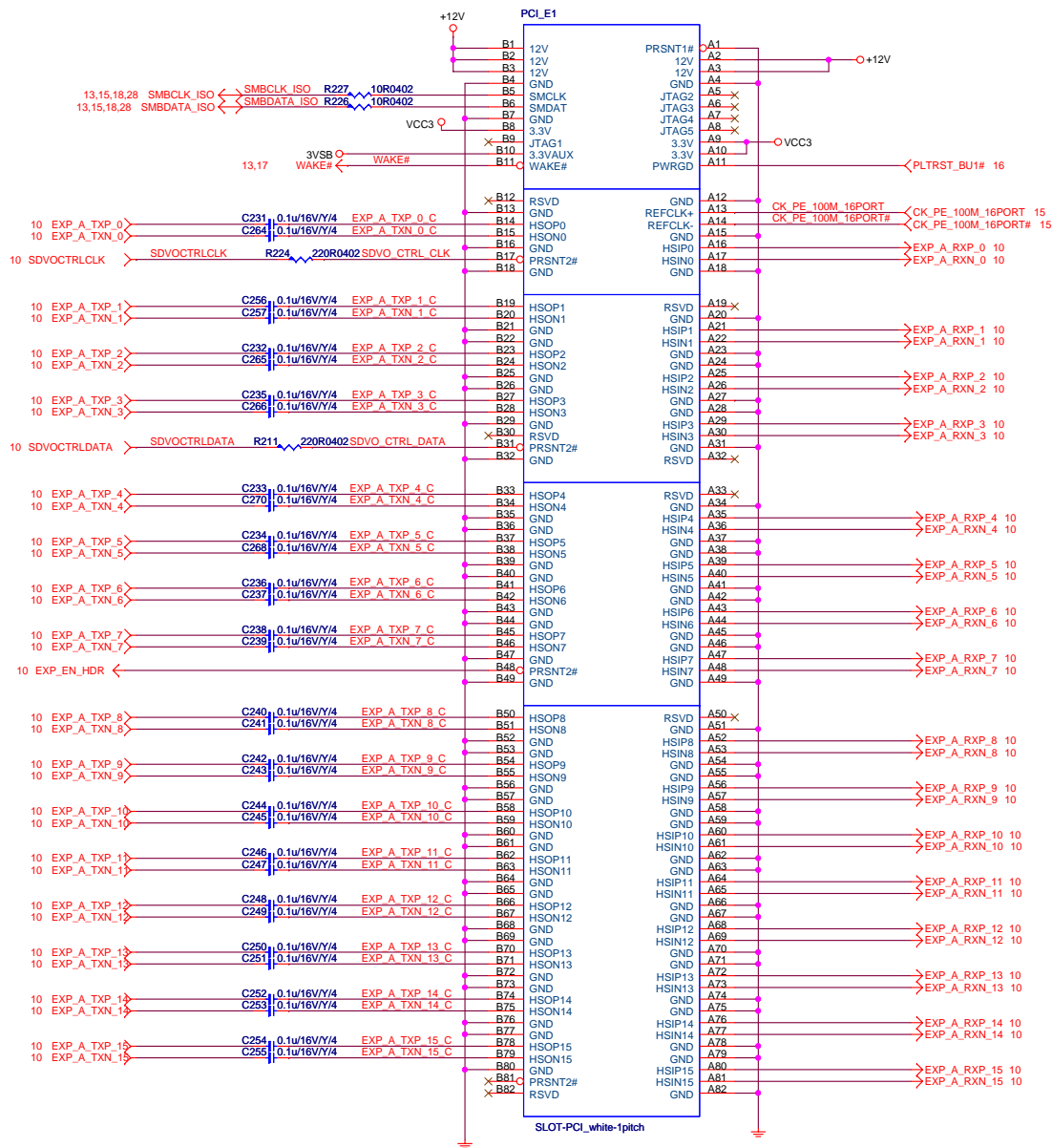


MICRO-STAR INT'L CO.,LTD

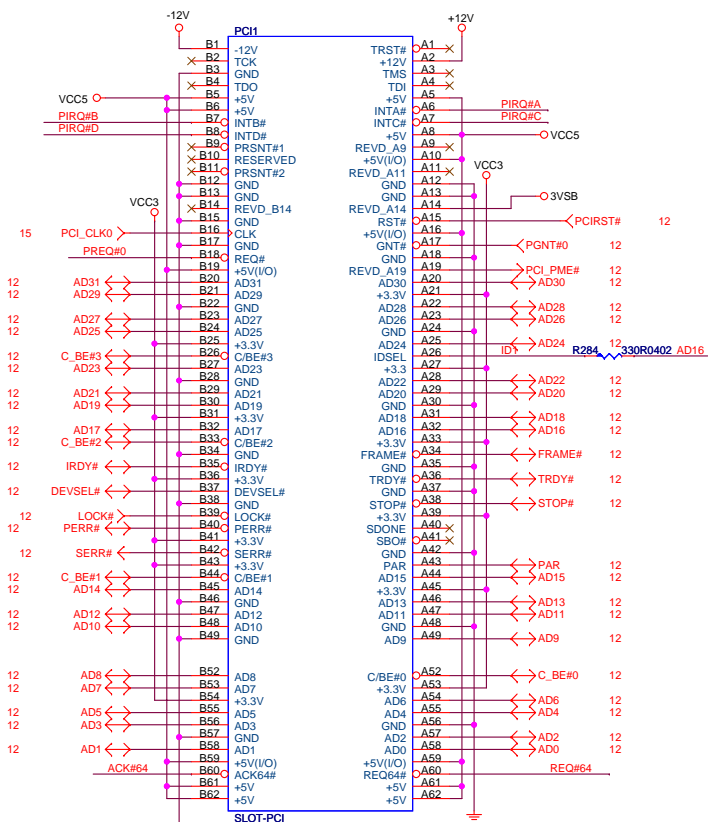
MS-7398

Size	Document Description	Rev
Custom	DDR II VTT DECOUPLING	0A
Date:	Tuesday, July 31, 2007	Sheet 20 of 32



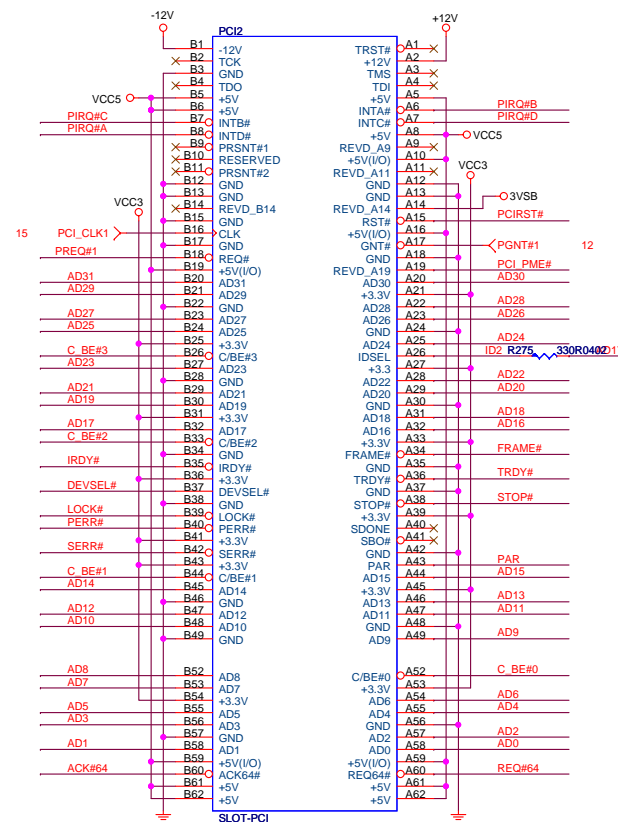


PCI SLOT 1 (PCI VER: 2.2 COMPLY)



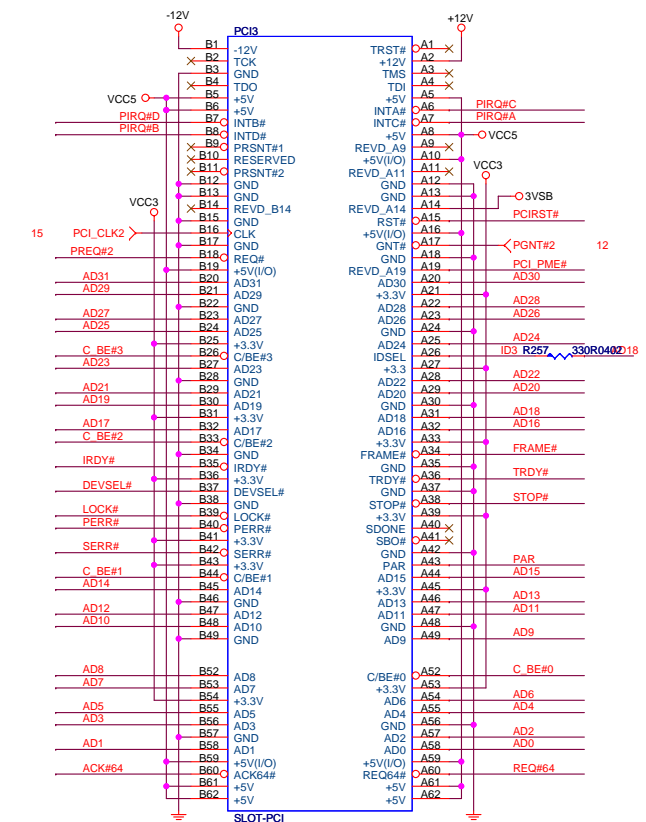
IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

PCI SLOT 2 (PCI VER: 2.2 COMPLY)



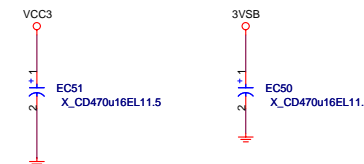
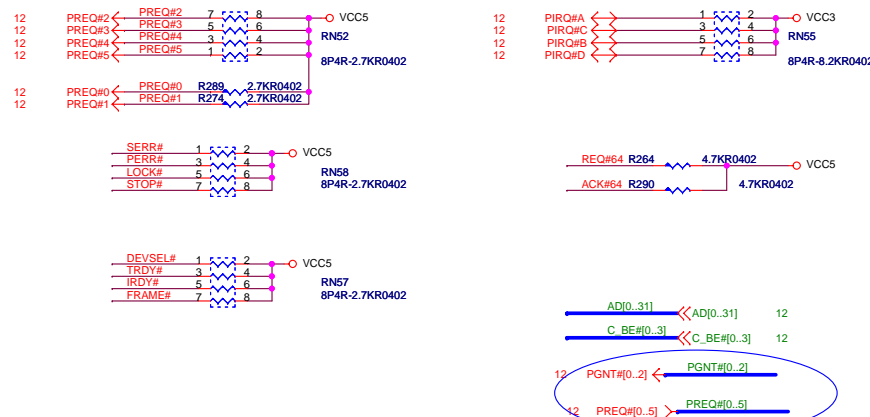
IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

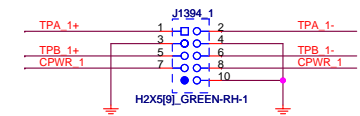
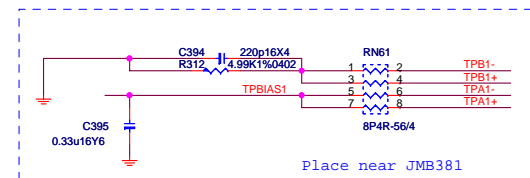
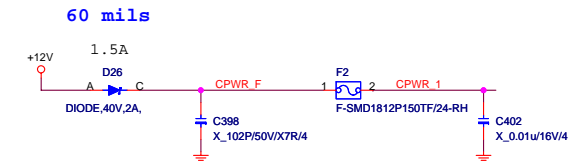
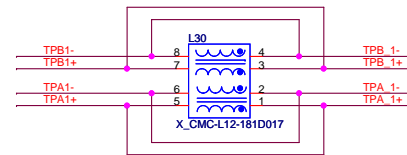
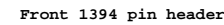
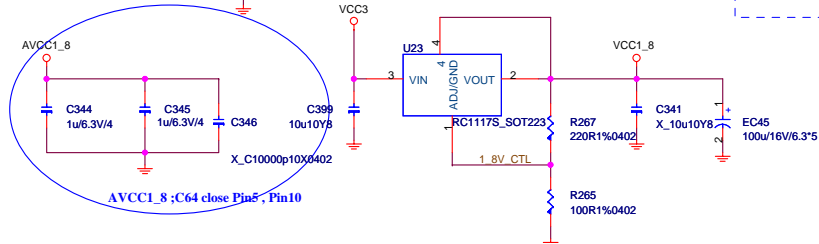
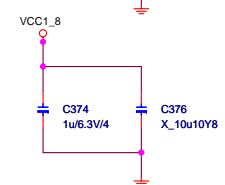
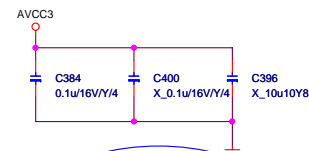
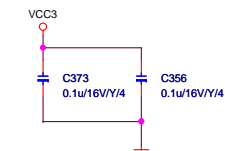
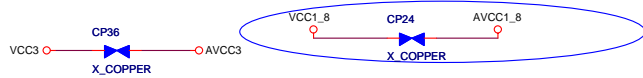
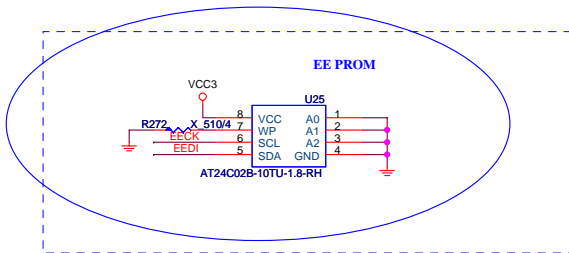
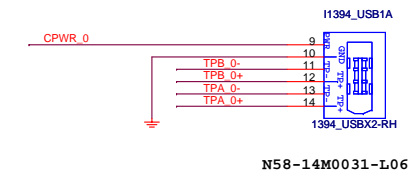
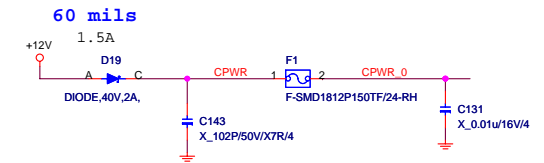
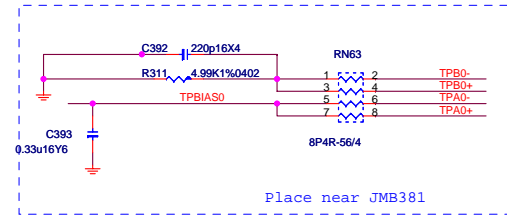
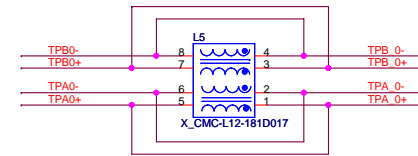
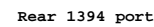
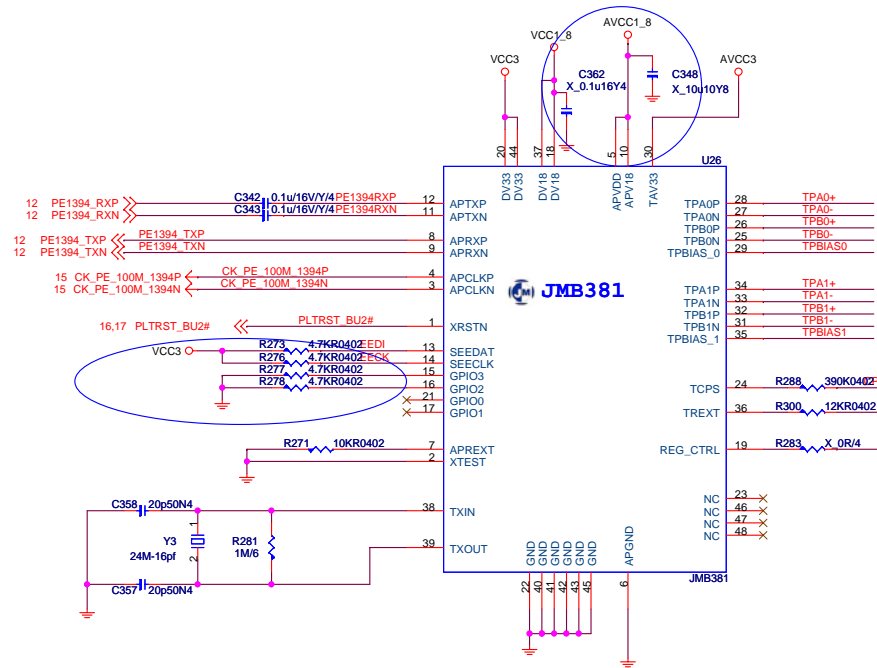
PCI SLOT 2 (PCI VER: 2.2 COMPLY)



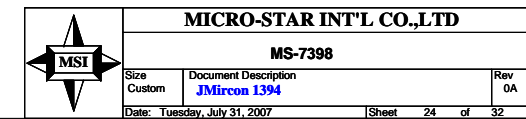
IDSEL = AD18
MASTER = PREQ#2
PIRQ#C

PCI PULL-UP / DOWN RESISTORS

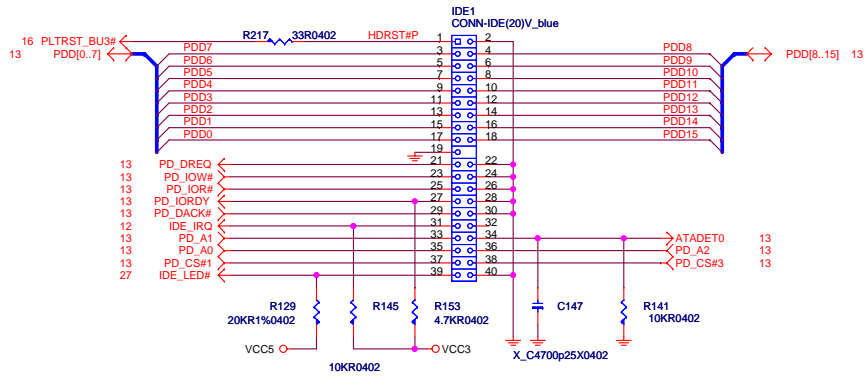




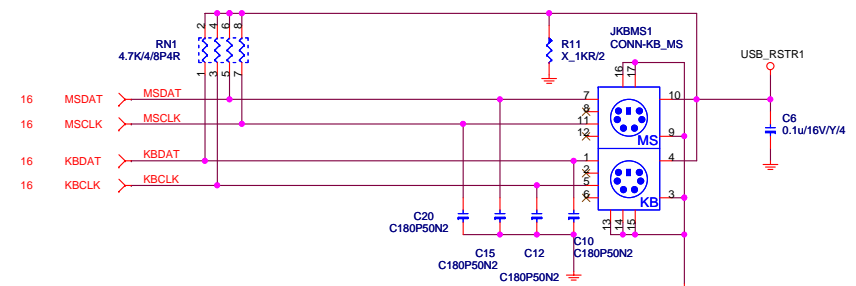
For Intel 1394 pinheader



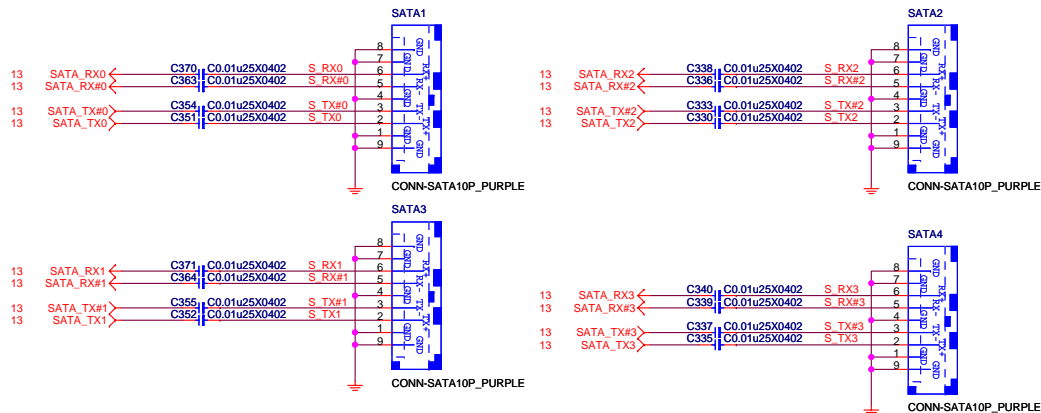
ATA 33/66/100 IDE Connectors



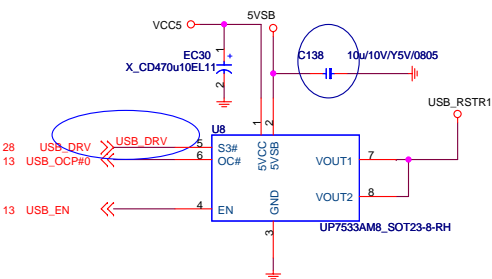
PS2 KEYBOARD & MOUSE CONNECTOR



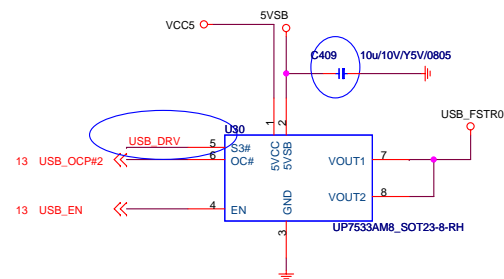
SERIAL ATA CONNECTOR BLOCK



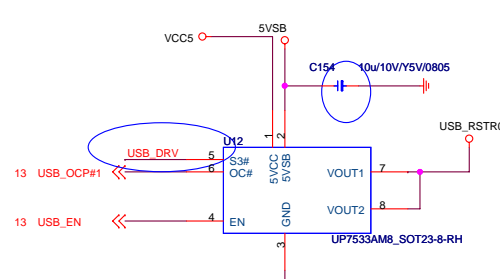
POWER CIRCUIT FOR USB PORT 0,1



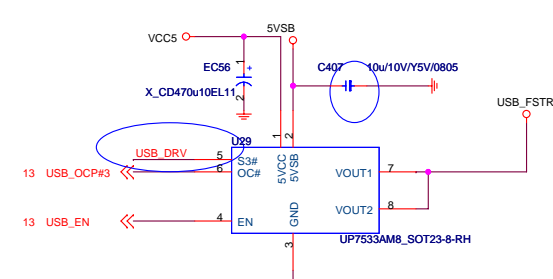
POWER CIRCUIT FOR USB PORT 4,5



POWER CIRCUIT FOR USB PORT 2,3

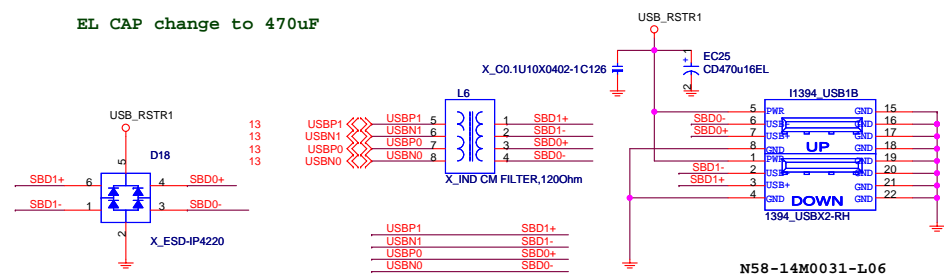


POWER CIRCUIT FOR USB PORT 6,7



REAR PANEL USB CONNECTOR FOR USB PORT 0,1

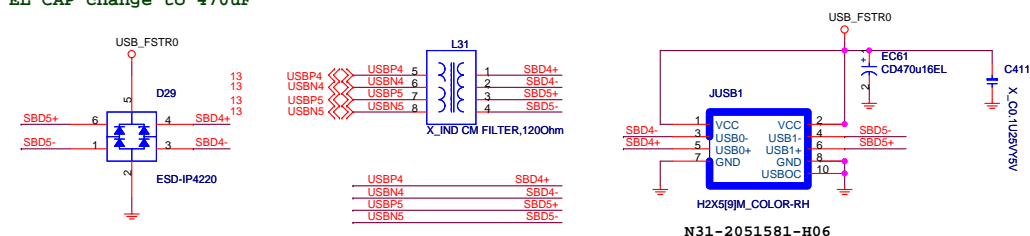
EL CAP change to 470uF



22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

FRONT PANEL USB CONNECTOR FOR USB PORT 4,5

EL CAP change to 470uF

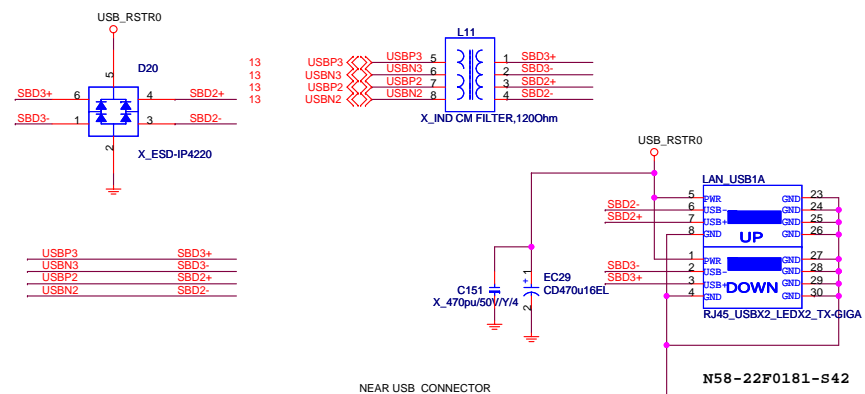


22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

EL CAP change to 470uF

REAR PANEL USB CONNECTOR FOR USB PORT 2,3

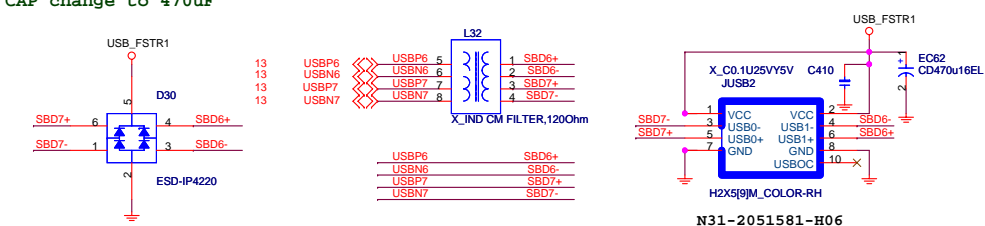
Stuff for channel and gateway



22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

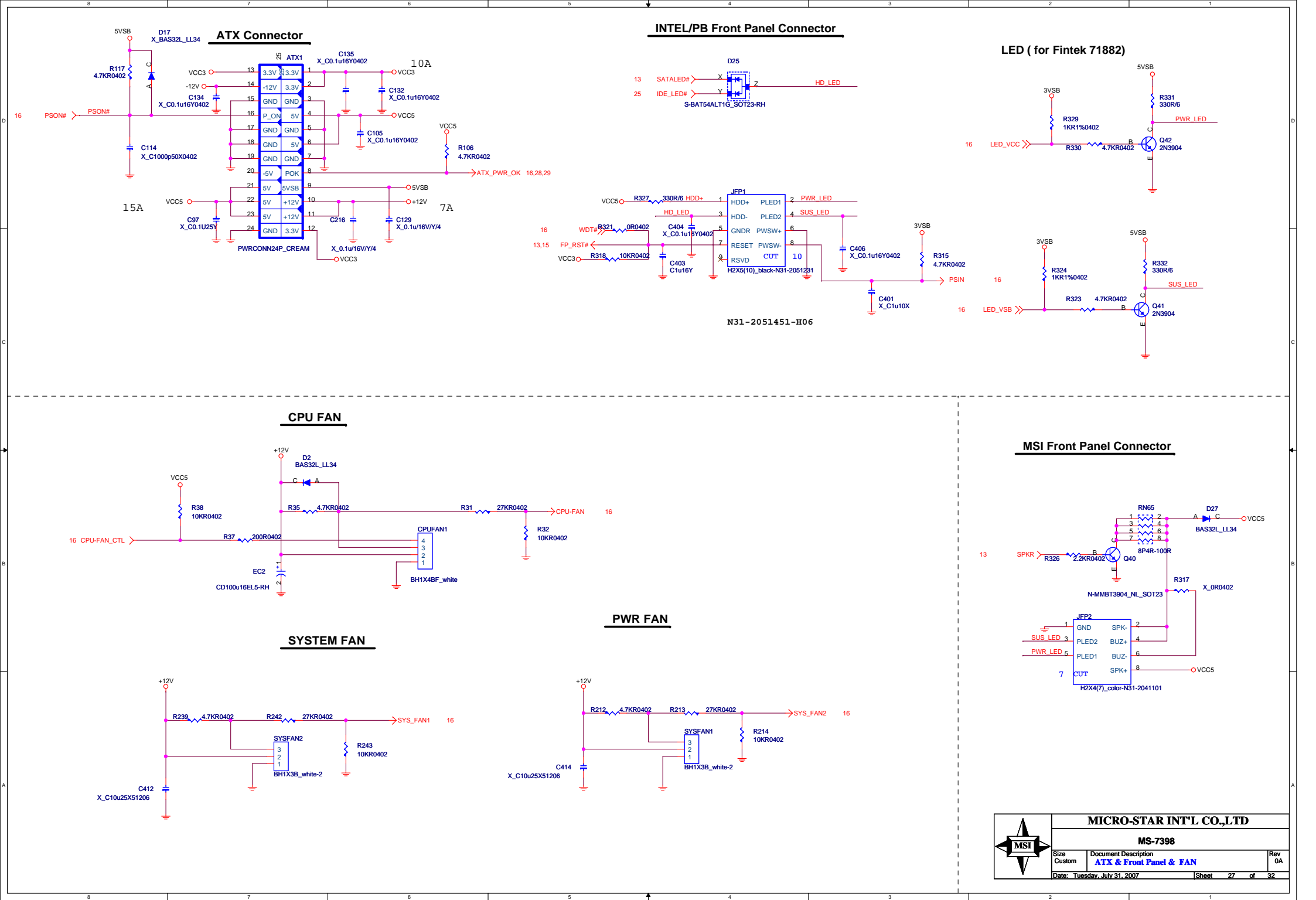
FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

EL CAP change to 470uF

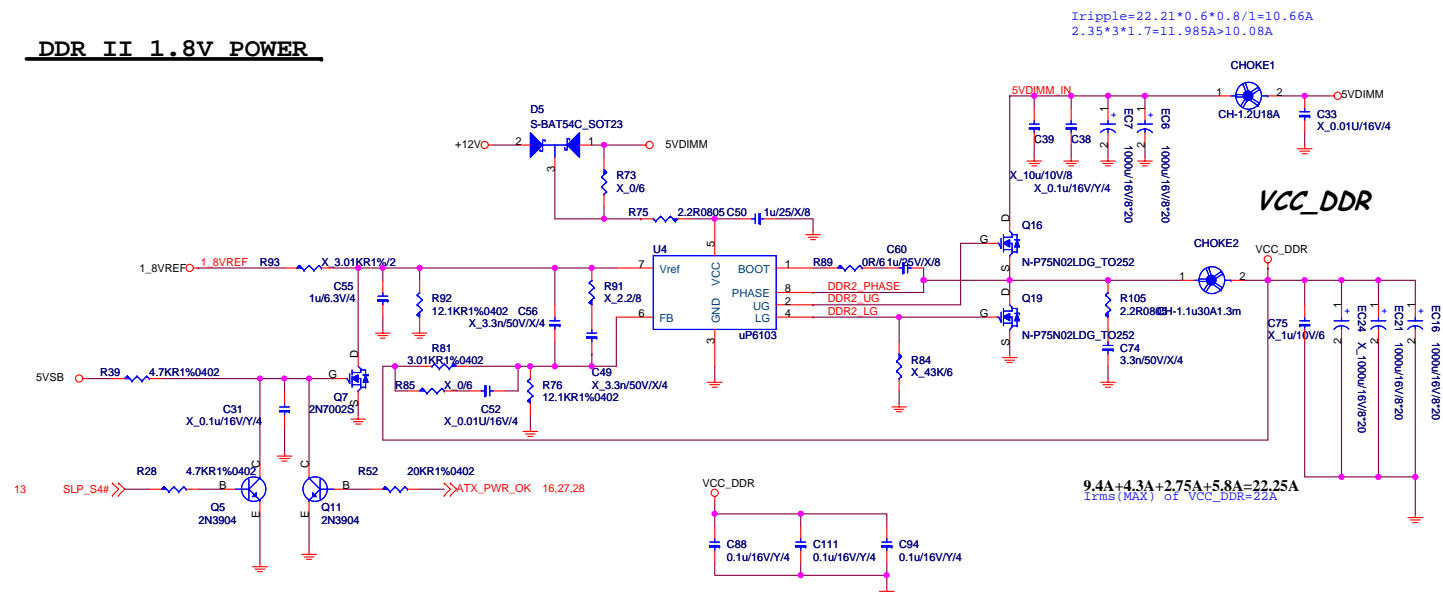


22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

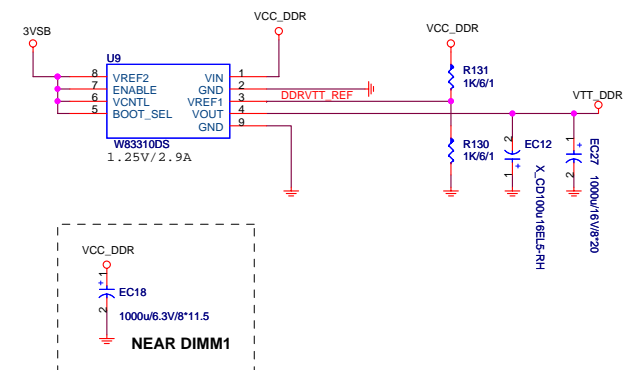
MICRO-STAR INT'L CO.,LTD		
MS-7398		
Size	Document Description	Rev
Custom	USB CONNECTORS	0A
Date: Tuesday, July 31, 2007		Sheet 26 of 32



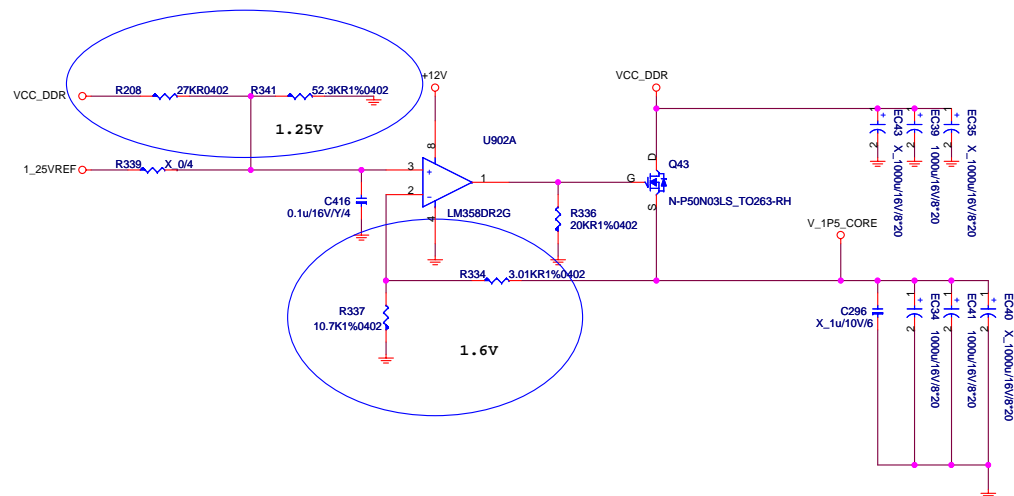
DDR II 1.8V POWER



DDR VTT Power



NB 1.5V POWER



$$\text{Tripple} = 16.3 \times 0.49 \times 0.878 / 1 = 7A$$

$$1.14 \times 3 \times 1.7 = 5.814A > 5.59A$$

NB_V1.5

$I_{rms}(MAX)$ of V_1P5_CORE

$$13.8A + 6.2A = 20A$$



MICRO-STAR INT'L CO.,LTD

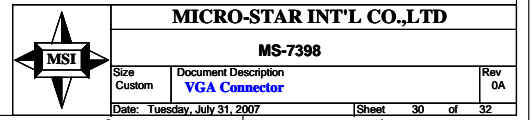
MS-7398

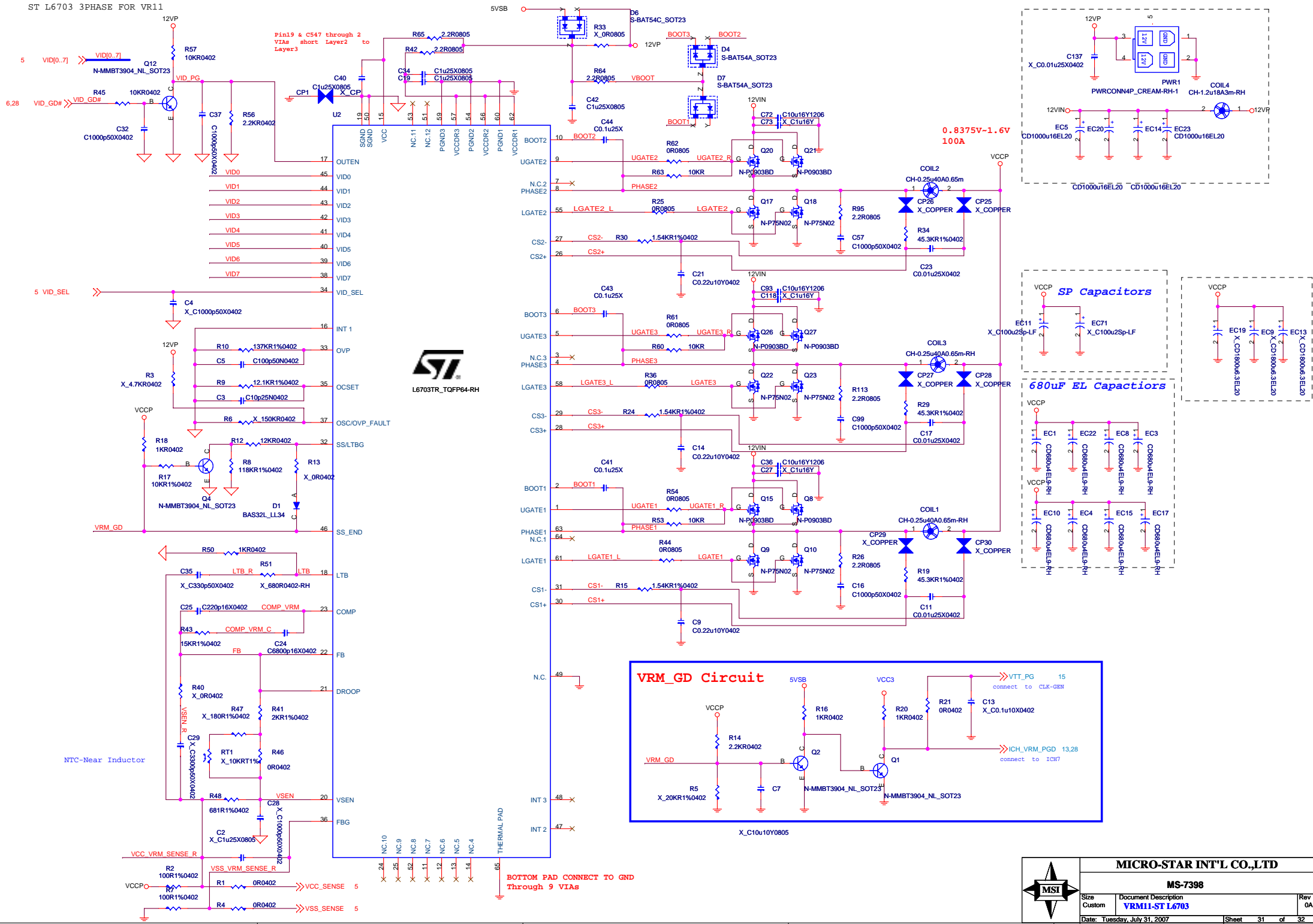
Size	Document Description	Rev
Custom	NB Core Power & DDR Power	0A
Date: Tuesday, July 31, 2007	Sheet 29 of 32	

PLACE CLOSE TO VGA CONNECTOR

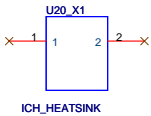
as close as possible to VGA connector
within 0.5 inch — — —

N51-15F0391-F02

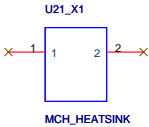




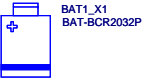
ICH7 HEATSINK



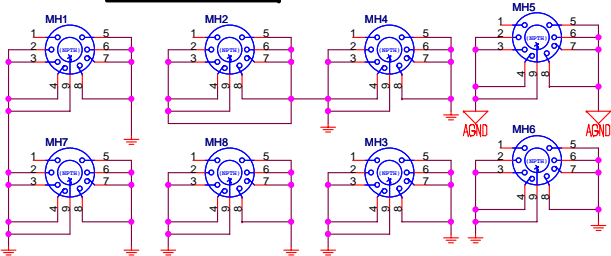
MCH HEATSINK



EMI



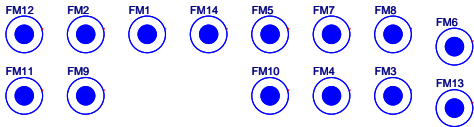
Mounting Holes



Simulation



Optics Orientation Holes



Opt-part
Opt-part
<div><div>U801</div><div>AUDIO 3孔</div></div> <div>JACK-AUDIOX3F_PK/GR/BU-RH-2</div>